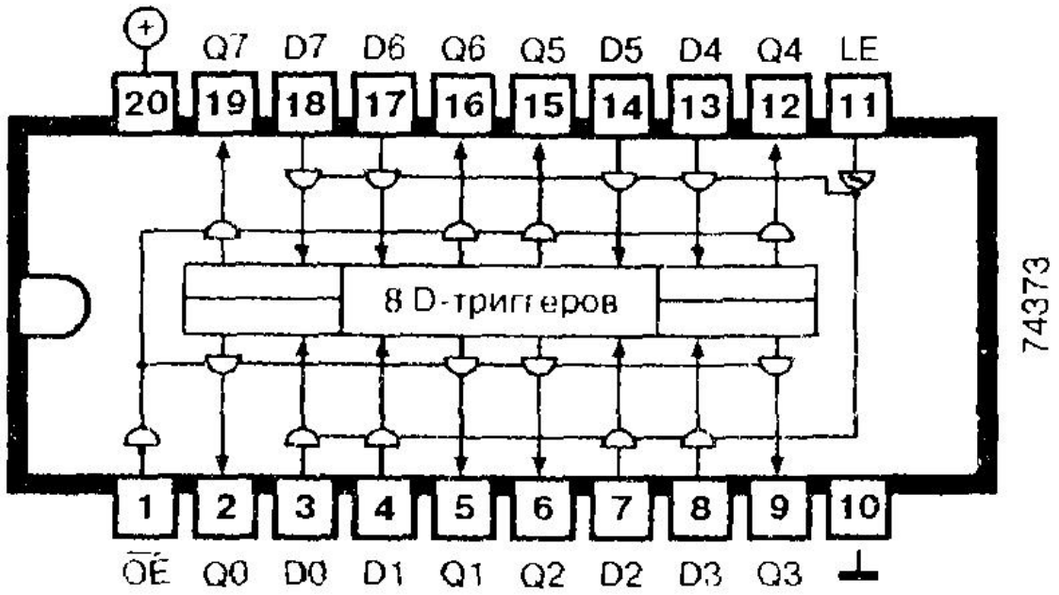
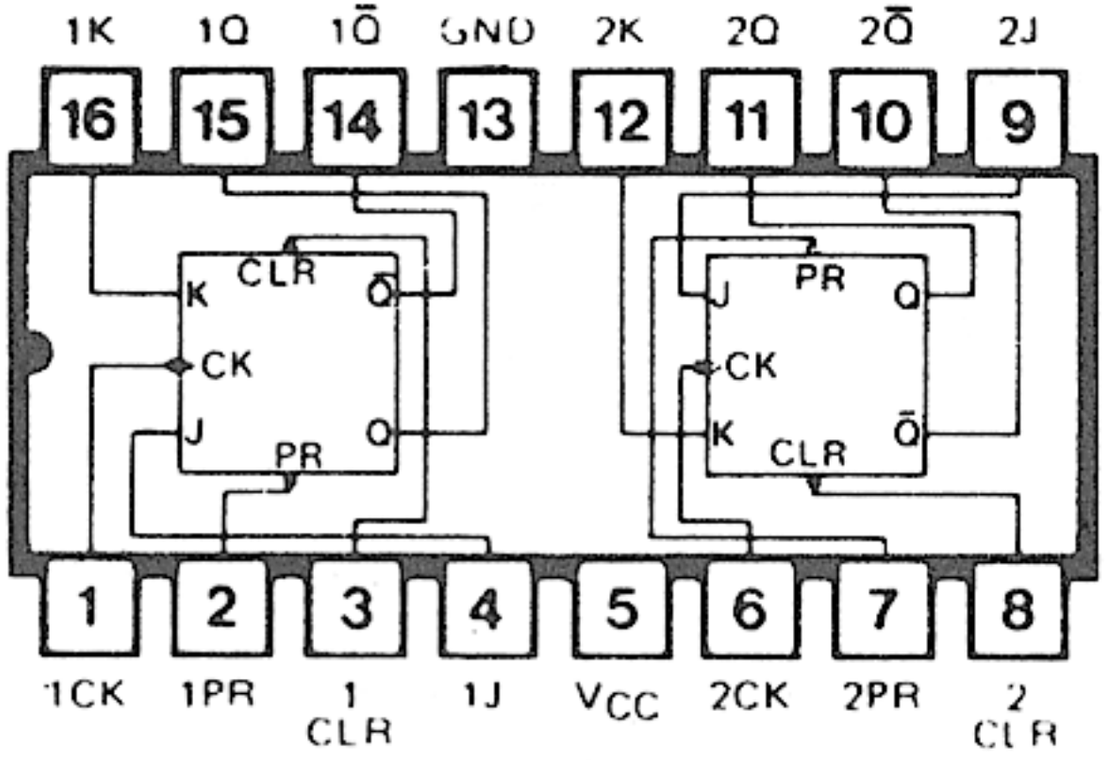
Biestáveis

Parâmetros Elétricos & Exercícios

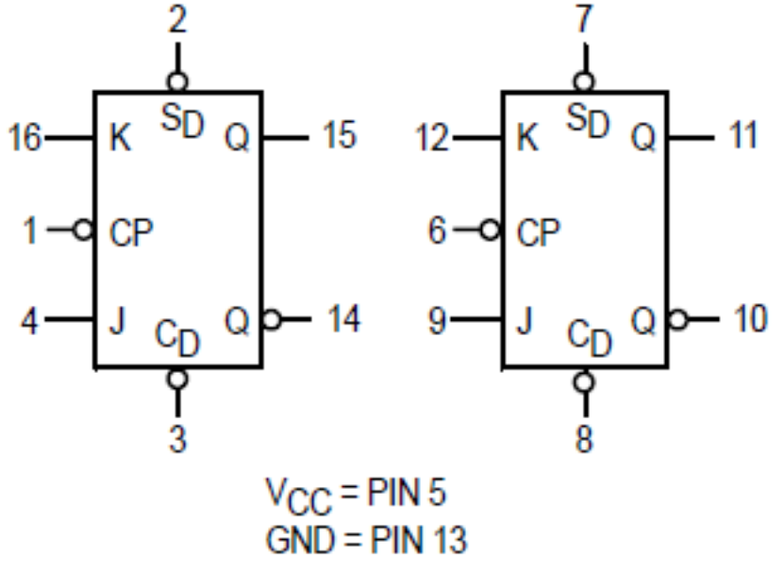
Prof. Fernando Passold

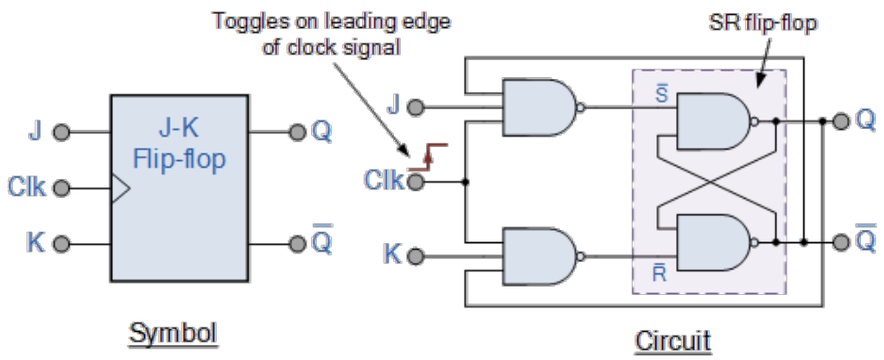
Circuitos Digitais II

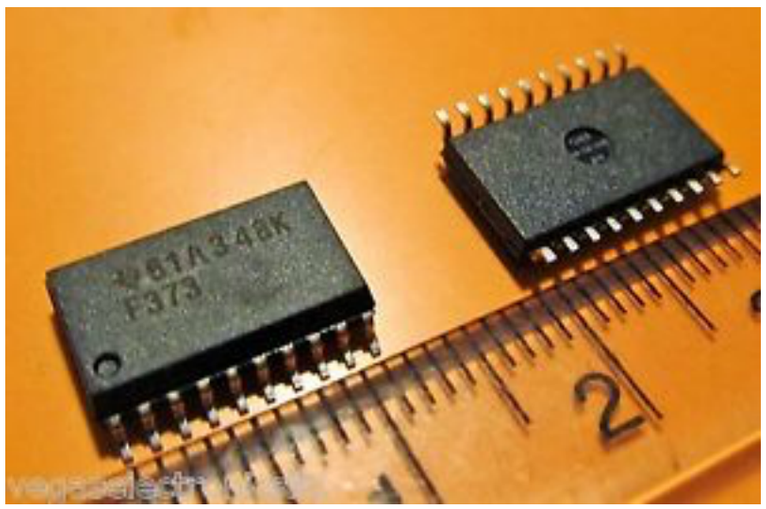




LOGIC SYMBOL







BIESTÁVEIS COMERCIAIS

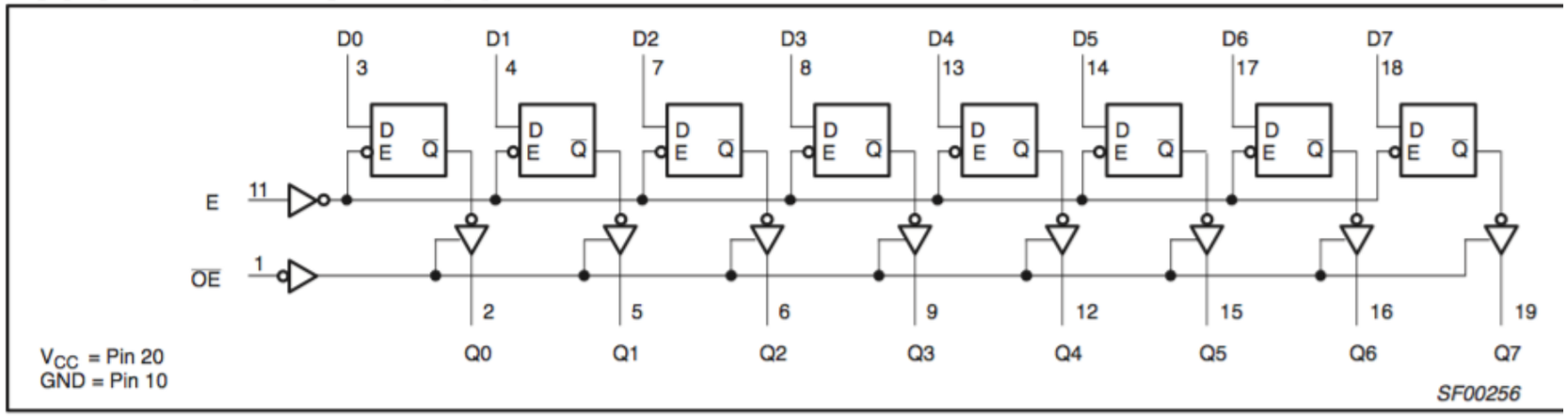
Detalhes

Fernando Passold

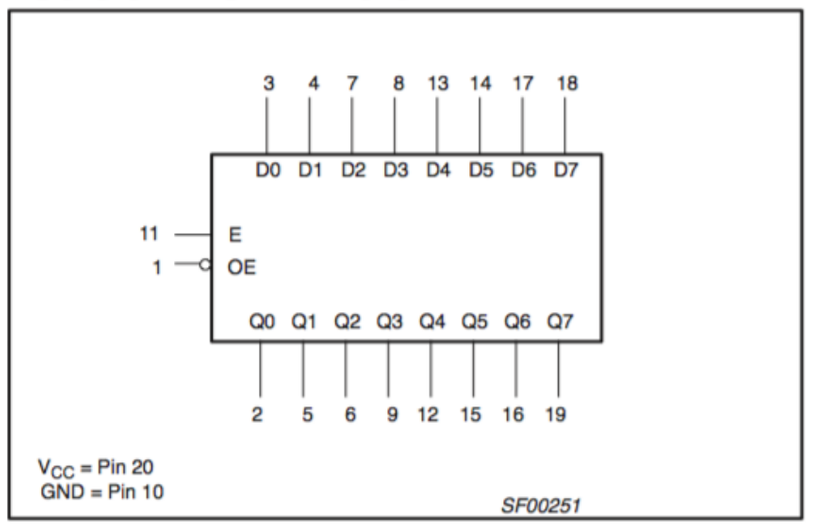
74F373

Octal transparent latch (3-State)

LOGIC DIAGRAM FOR 74F373



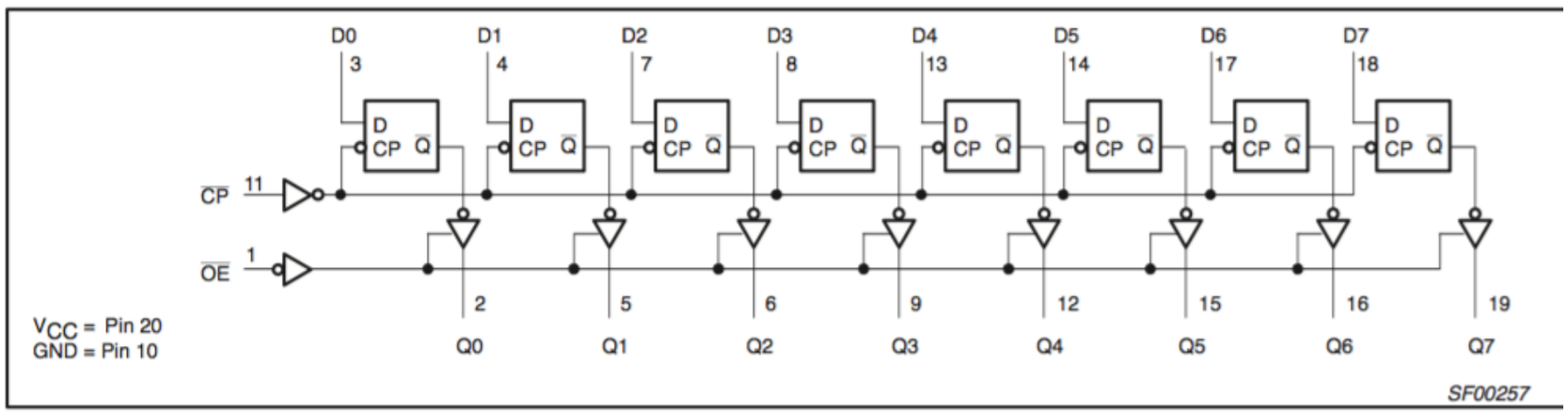
LOGIC SYMBOL – 74F373



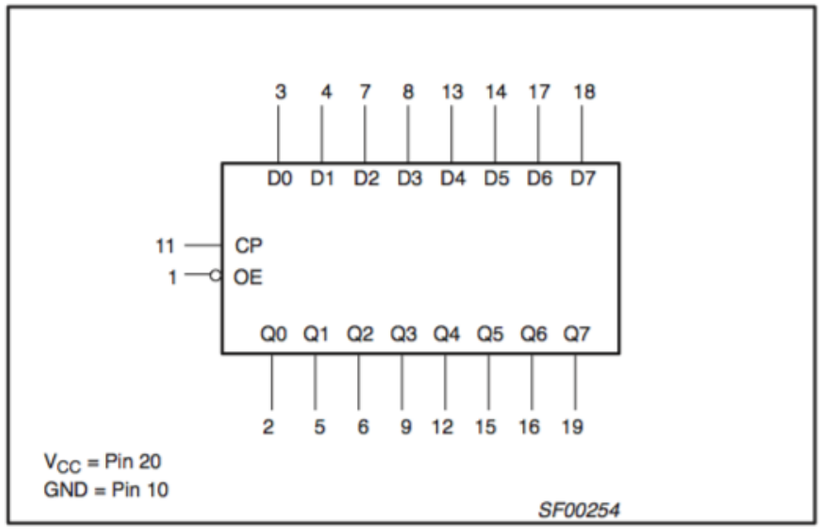
74F374

Octal D flip-flop (3-State)

LOGIC DIAGRAM FOR 74F374



IEC/IEE SYMBOL – 74F374



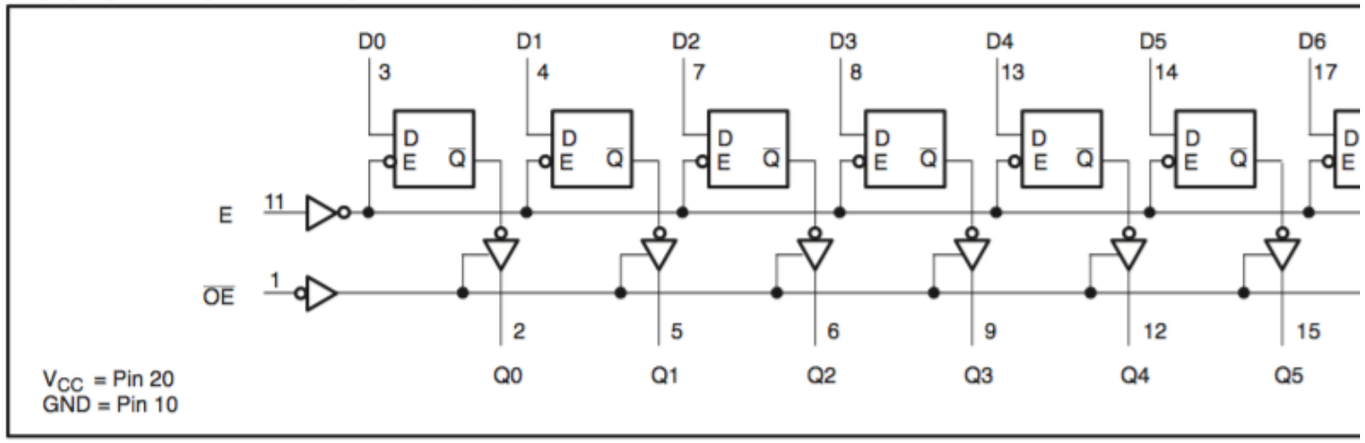
Obs:

Saídas em 3o-estado (Common 3-State output register);

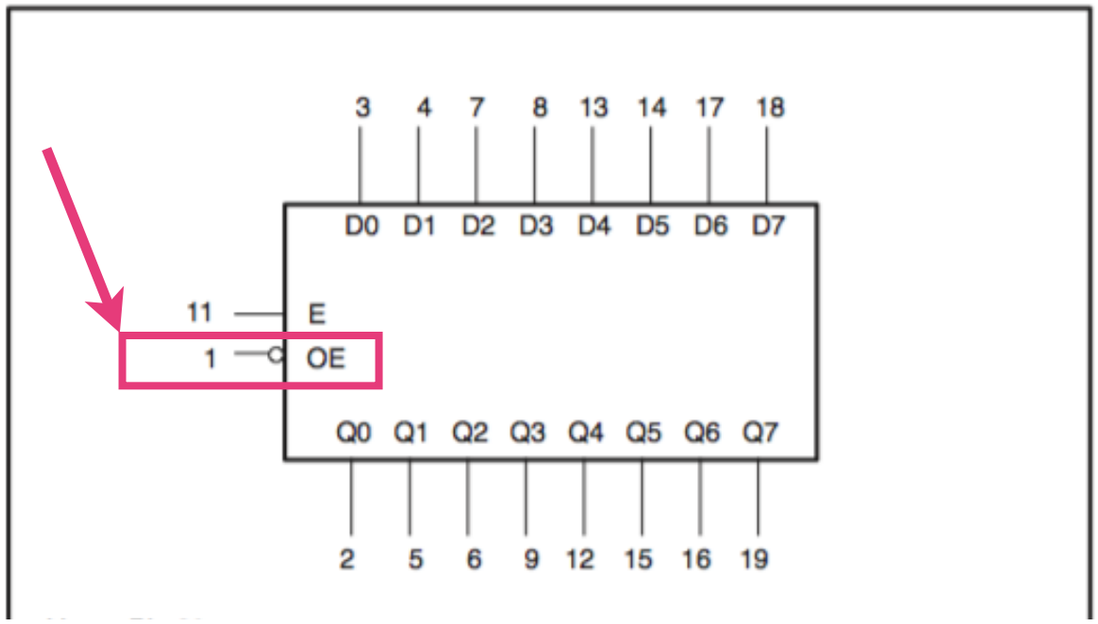
74F373

Octal transparent latch (3-State)

LOGIC DIAGRAM FOR 74F373



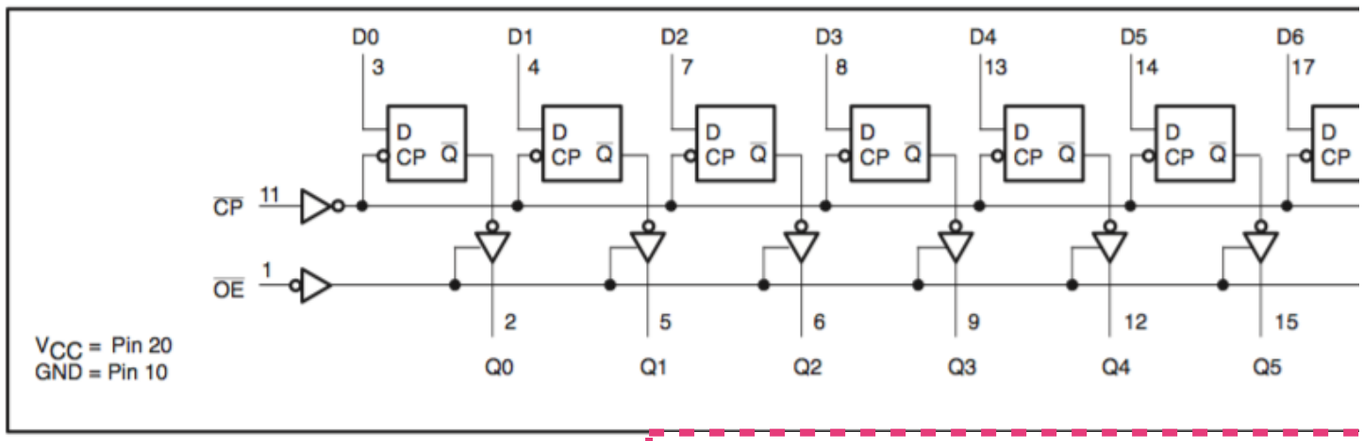
LOGIC SYMBOL – 74F373



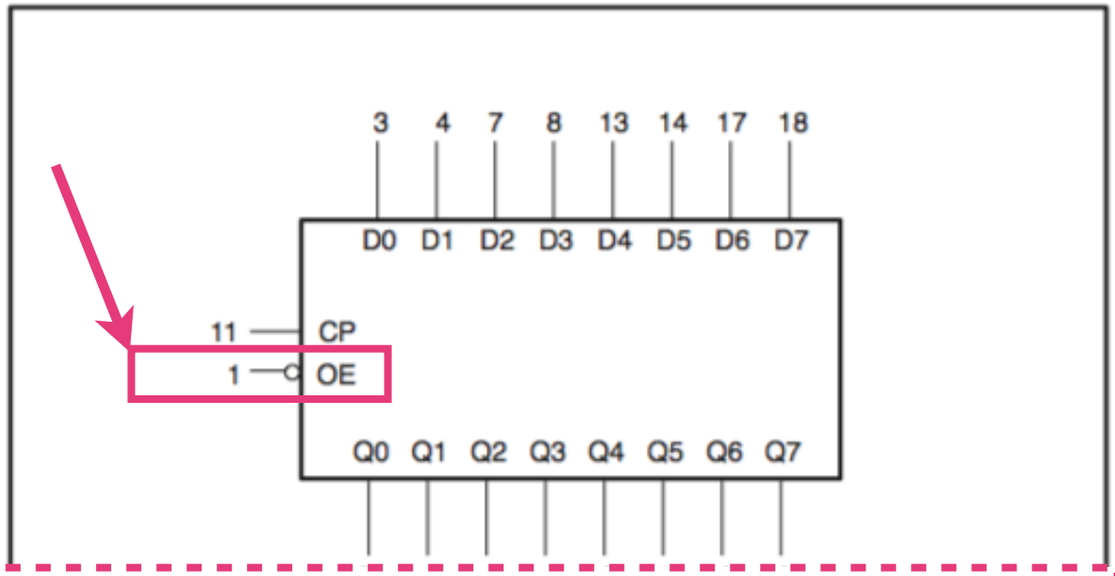
74F374

Octal D flip-flop (3-State)

LOGIC DIAGRAM FOR 74F374



IEC/IEE SYMBOL – 74F374



Obs:
Saídas em 3o-estado (Commor

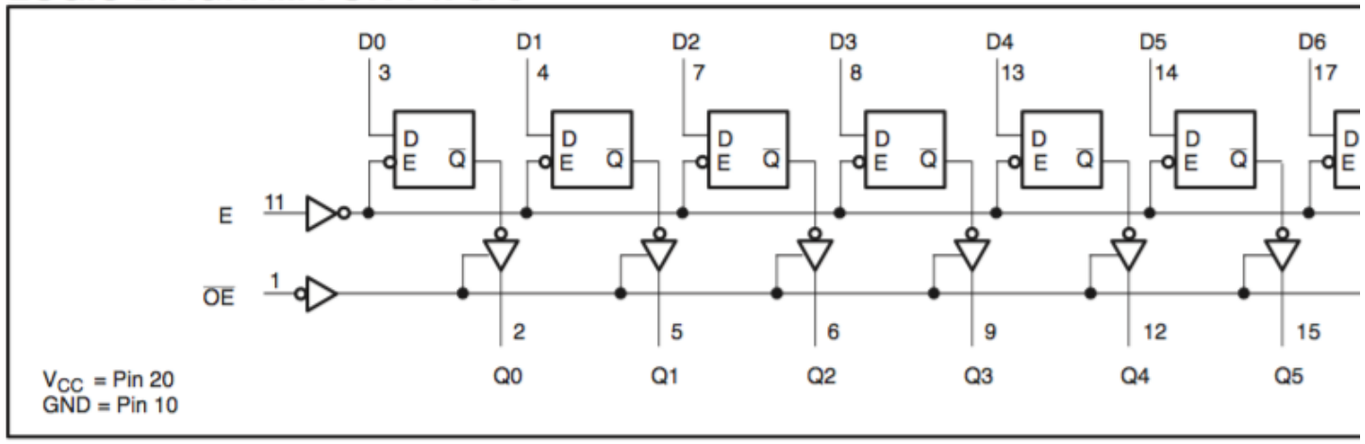
The active-LOW output enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

74F373

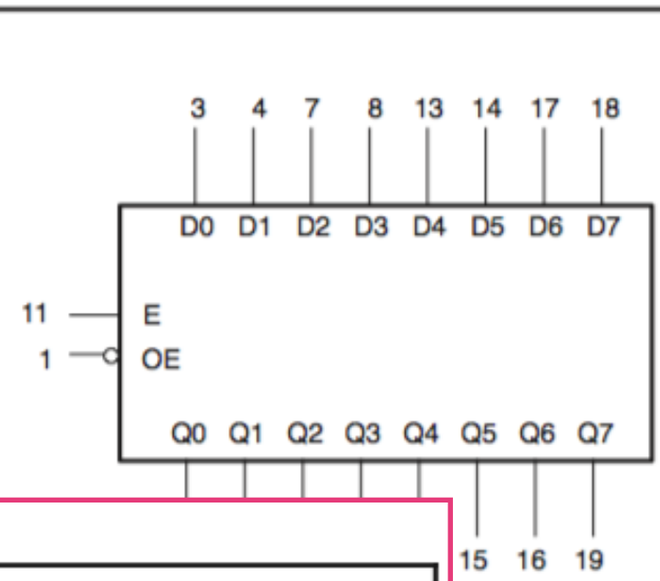
Octal transparent latch (3-State)

PHILIPS

LOGIC DIAGRAM FOR 74F373



LOGIC SYMBOL – 74F373



SF00251

FUNCTION TABLE FOR 74F373

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn		Q0 - Q7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

NOTES:

H = High-voltage level
h = HIGH state must be present one set-up time before the HIGH-to-LOW enable transition
L = Low-voltage level
l = LOW state must be present one set-up time before the HIGH-to-LOW enable transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = HIGH-to-LOW enable transition

The active-LOW output enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

PHILIPS

FUNCTION TABLE FOR 74F374

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	Q0 – Q7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↓	X	NC	NC	Hold
H	↓	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

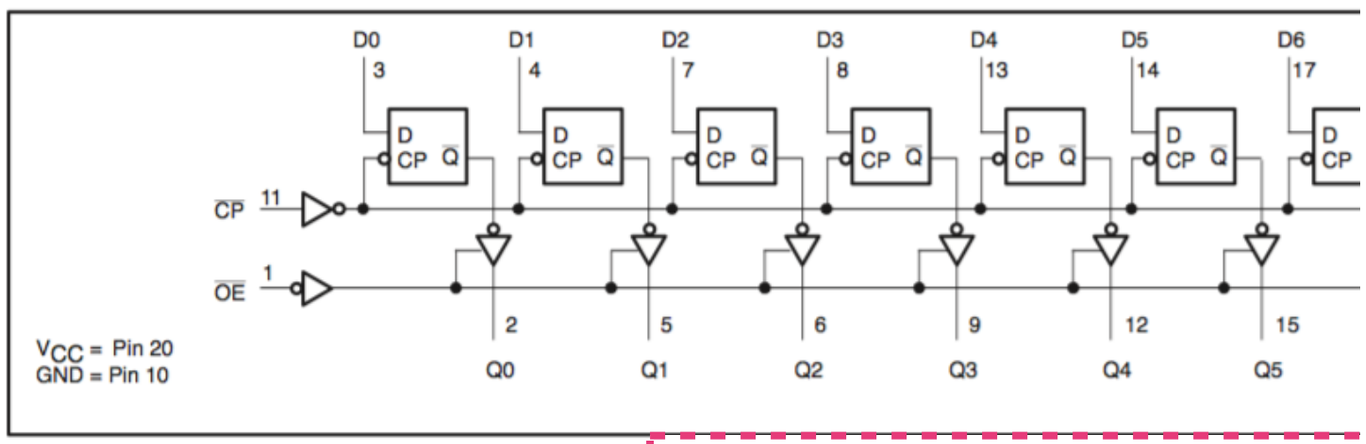
NOTES:

H = High-voltage level
h = HIGH state must be present one set-up time before the LOW-to-HIGH clock transition
L = Low-voltage level
l = LOW state must be present one set-up time before the LOW-to-HIGH clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = LOW-to-HIGH clock transition
↓ = Not LOW-to-HIGH clock transition

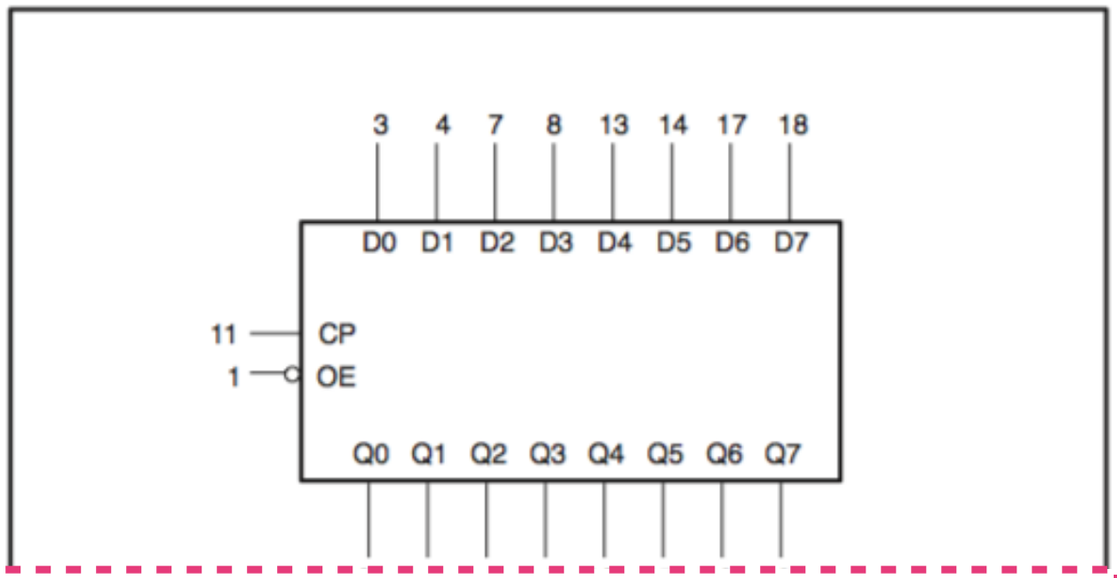
74F374

Octal D flip-flop (3-State)

LOGIC DIAGRAM FOR 74F374



IEC/IEE SYMBOL – 74F374



Obs:
Saídas em 3o-estado (Commor

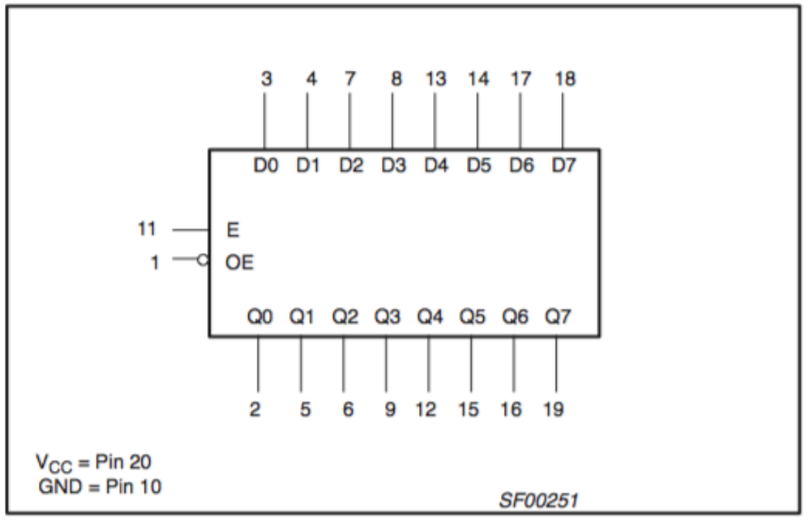
The active-LOW output enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

PHILIPS

74F373

Octal transparent latch (3-State)

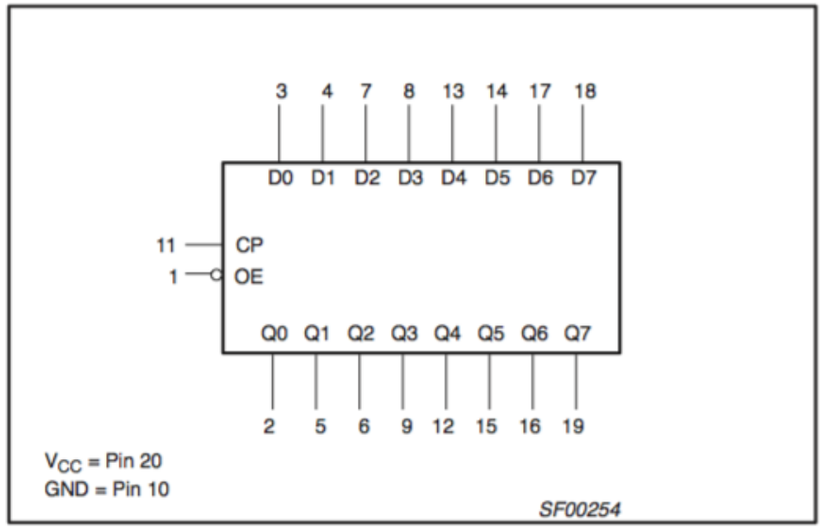
LOGIC SYMBOL – 74F373



74F374

Octal D flip-flop (3-State)

IEC/IEE SYMBOL – 74F374



DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

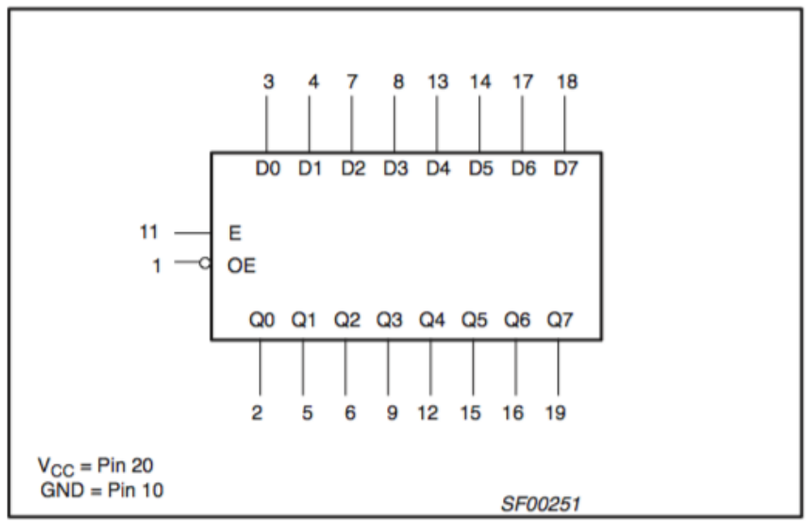
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0 V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5 V				–0.6	mA
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7 V				50	µA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.5 V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	74F373	V_{CC} = MAX			35	60	mA
		74F374				57	86	mA

NOTES:

74F373

Octal transparent latch (3-State)

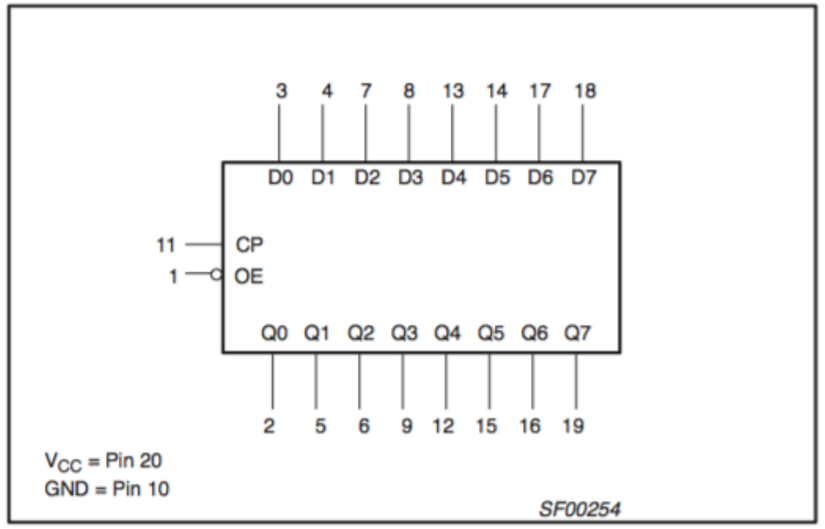
LOGIC SYMBOL – 74F373



74F374

Octal D flip-flop (3-State)

IEC/IEE SYMBOL – 74F374



AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS: T_{amb} = +25 °C, V_{CC} = +5.0 V, C_L = 50 pF; R_L = 500 Ω			LIMITS: T_{amb} = 0 °C to +70 °C, V_{CC} = +5.0 V ± 10%, C_L = 50 pF; R_L = 500 Ω		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn		Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	12.0 8.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	11.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.0 6.0	ns
f_{max}	Maximum clock frequency	74F374	Waveform 1	150	165		140		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	3.5 3.5	5.0 5.0	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.0 7.5	2.0 2.0	12.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	6.0 5.5	2.0 2.0	7.0 6.5	ns

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25 °C, V_{CC} = +5.0 V, C_L = 50 pF; R_L = 500 Ω			T_{amb} = 0 °C to +70 °C, V_{CC} = +5.0 V ± 10%, C_L = 50 pF; R_L = 500 Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn		Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	12.0 8.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	11.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.0 6.0	ns
f_{max}	Maximum clock frequency	74F374	Waveform 1	150	165		140		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	3.5 3.5	5.0 5.0	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.0 7.5	2.0 2.0	12.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	6.0 5.5	2.0 2.0	7.0 6.5	ns

AC SET-UP REQUIREMENTS

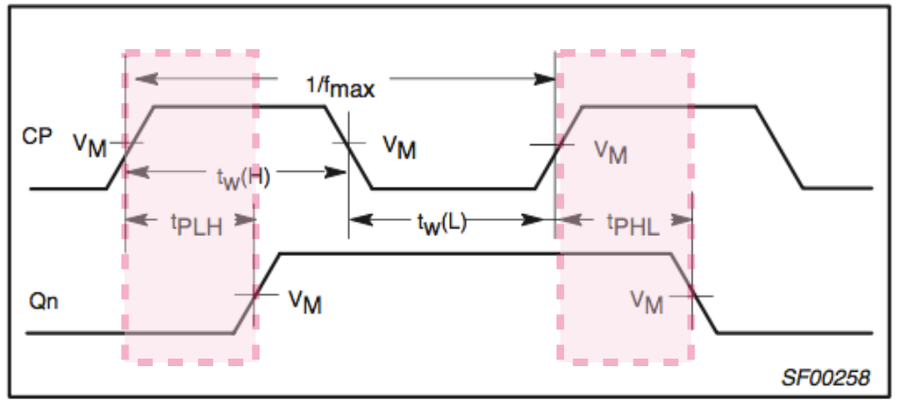
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25 °C, V_{CC} = +5.0 V, C_L = 50 pF, R_L = 500 Ω			T_{amb} = 0 °C to +70 °C, V_{CC} = +5.0 V ± 10%, C_L = 50 pF, R_L = 500 Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Set-up time, HIGH or LOW level Dn to E	74F373	Waveform 4	0 1.0			0 1.0		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW level Dn to E		Waveform 4	3.0 3.0			3.0 3.0		ns
t_w (H)	E Pulse width, HIGH		Waveform 1	3.5			4.0		ns
t_{su} (H) t_{su} (L)	Set-up time, HIGH or LOW level Dn to CP	74F374	Waveform 5	2.0 2.0			2.0 2.0		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW level Dn to CP		Waveform 5	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, HIGH or LOW		Waveform 5	3.5 4.0			3.5 4.0		ns

AC ELECTRICAL CHARACTERISTICS

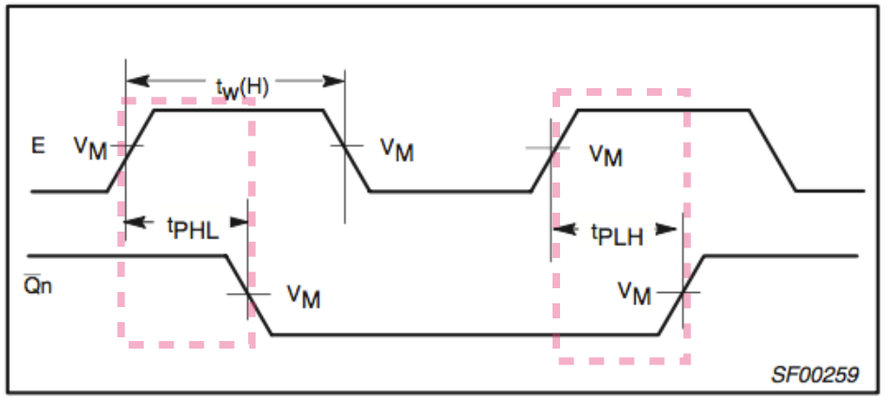
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25 °C, V_{CC} = +5.0 V, C_L = 50 pF; R_L = 500 Ω			T_{amb} = 0 °C to +70 °C, V_{CC} = +5.0 V ± 10%, C_L = 50 pF; R_L = 500 Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn		Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	12.0 8.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	11.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.0 6.0	ns
f_{max}	Maximum clock frequency	74F374	Waveform 1	150	165		140		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	3.5 3.5	5.0 5.0	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.0 7.5	2.0 2.0	12.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	6.0 5.5	2.0 2.0	7.0 6.5	ns

AC SET-UP REQUIREMENTS

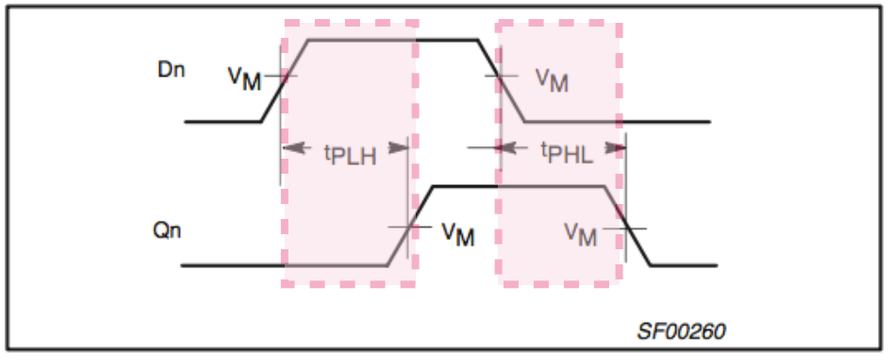
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25 °C, V_{CC} = +5.0 V, C_L = 50 pF, R_L = 500 Ω			T_{amb} = 0 °C to +70 °C, V_{CC} = +5.0 V ± 10%, C_L = 50 pF, R_L = 500 Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Set-up time, HIGH or LOW level Dn to E	74F373	Waveform 4	0 1.0			0 1.0		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW level Dn to E		Waveform 4	3.0 3.0			3.0 3.0		ns
t_w (H)	E Pulse width, HIGH		Waveform 1	3.5			4.0		ns
t_{su} (H) t_{su} (L)	Set-up time, HIGH or LOW level Dn to CP	74F374	Waveform 5	2.0 2.0			2.0 2.0		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW level Dn to CP		Waveform 5	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, HIGH or LOW		Waveform 5	3.5 4.0			3.5 4.0		ns



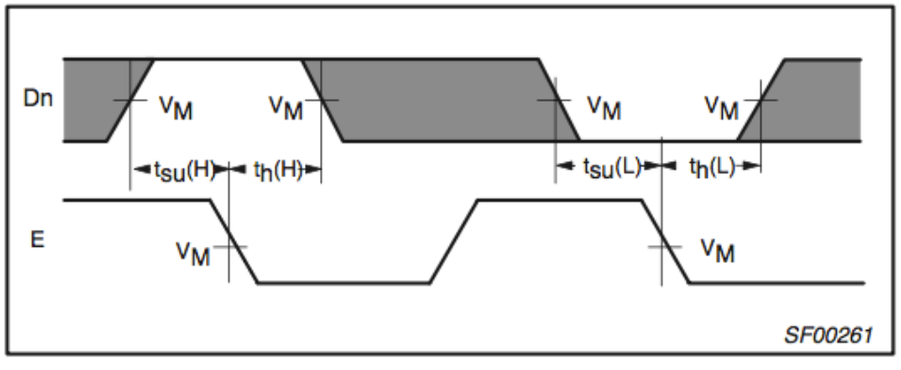
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency



Waveform 2. Propagation delay for enable to output and enable pulse width



Waveform 3. Propagation delay for data to output



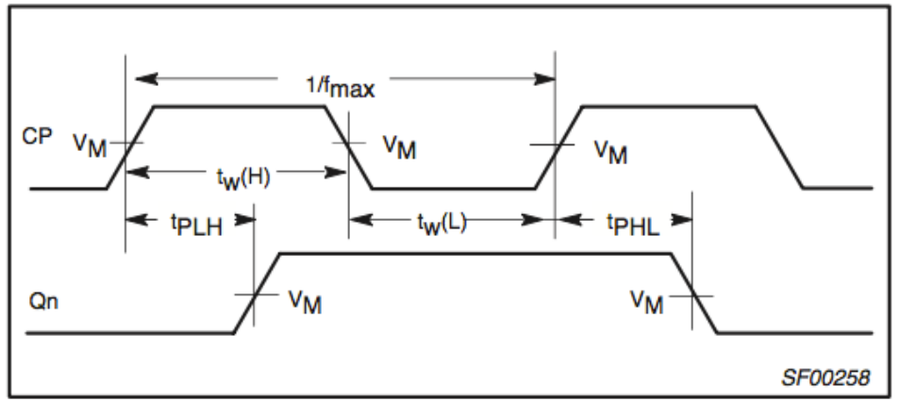
Waveform 4. Data set-up time and hold times

AC ELECTRICAL CHARACTERISTICS

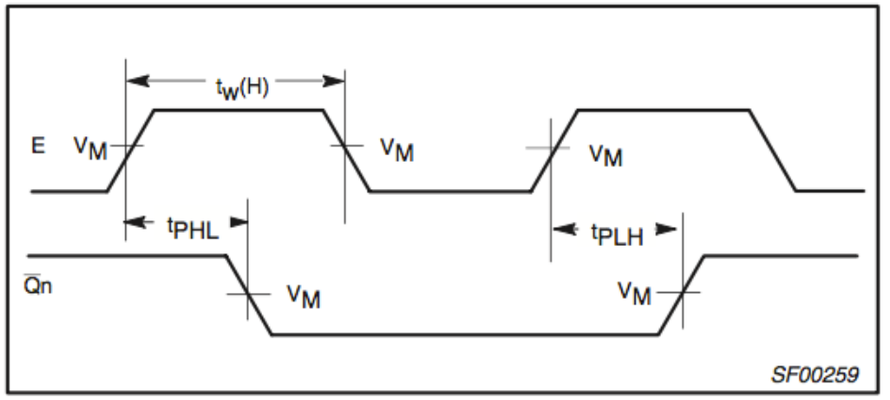
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25 °C, V_{CC} = +5.0 V, C_L = 50 pF; R_L = 500 Ω			T_{amb} = 0 °C to +70 °C, V_{CC} = +5.0 V ± 10%, C_L = 50 pF; R_L = 500 Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn		Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	12.0 8.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	11.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.0 6.0	ns
f_{max}	Maximum clock frequency	74F374	Waveform 1	150	165		140		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	3.5 3.5	5.0 5.0	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.0 7.5	2.0 2.0	12.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	6.0 5.5	2.0 2.0	7.0 6.5	ns

AC SET-UP REQUIREMENTS

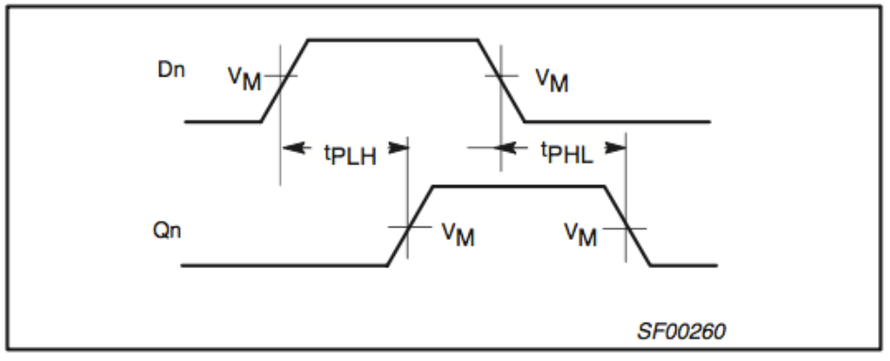
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25 °C, V_{CC} = +5.0 V, C_L = 50 pF, R_L = 500 Ω			T_{amb} = 0 °C to +70 °C, V_{CC} = +5.0 V ± 10%, C_L = 50 pF, R_L = 500 Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Set-up time, HIGH or LOW level Dn to E	74F373	Waveform 4	0 1.0			0 1.0		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW level Dn to E		Waveform 4	3.0 3.0			3.0 3.0		ns
t_w (H)	E Pulse width, HIGH		Waveform 1	3.5			4.0		ns
t_{su} (H) t_{su} (L)	Set-up time, HIGH or LOW level Dn to CP	74F374	Waveform 5	2.0 2.0			2.0 2.0		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW level Dn to CP		Waveform 5	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, HIGH or LOW		Waveform 5	3.5 4.0			3.5 4.0		ns



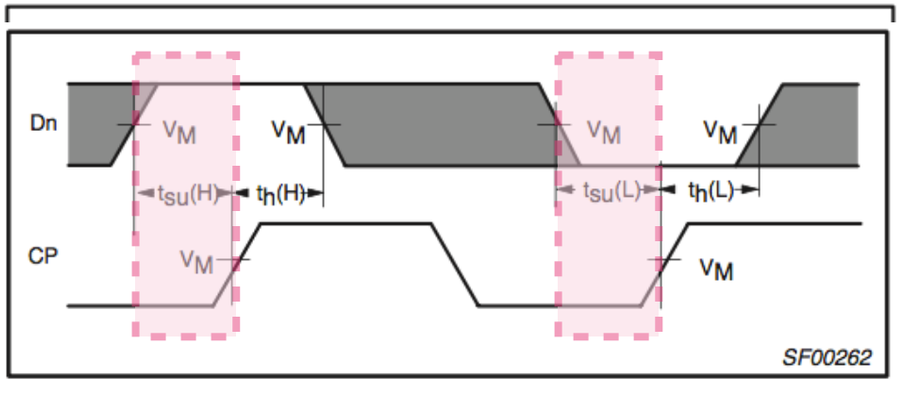
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency



Waveform 2. Propagation delay for enable to output and enable pulse width



Waveform 3. Propagation delay for data to output



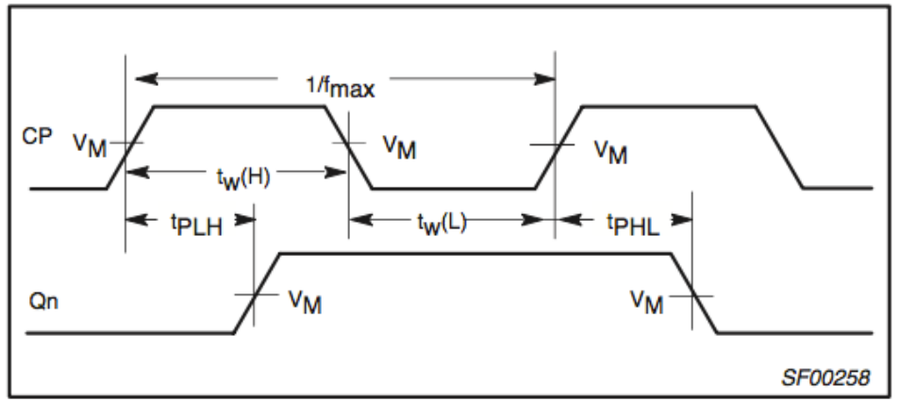
Waveform 5. Data set-up time and hold times

AC ELECTRICAL CHARACTERISTICS

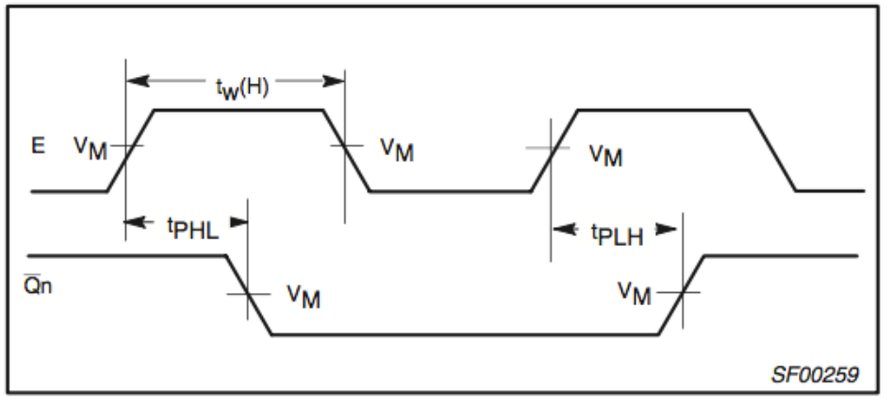
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25 °C, V_{CC} = +5.0 V, C_L = 50 pF; R_L = 500 Ω			T_{amb} = 0 °C to +70 °C, V_{CC} = +5.0 V ± 10%, C_L = 50 pF; R_L = 500 Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn		Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	12.0 8.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	11.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.0 6.0	ns
f_{max}	Maximum clock frequency	74F374	Waveform 1	150	165		140		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	3.5 3.5	5.0 5.0	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.0 7.5	2.0 2.0	12.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	6.0 5.5	2.0 2.0	7.0 6.5	ns

AC SET-UP REQUIREMENTS

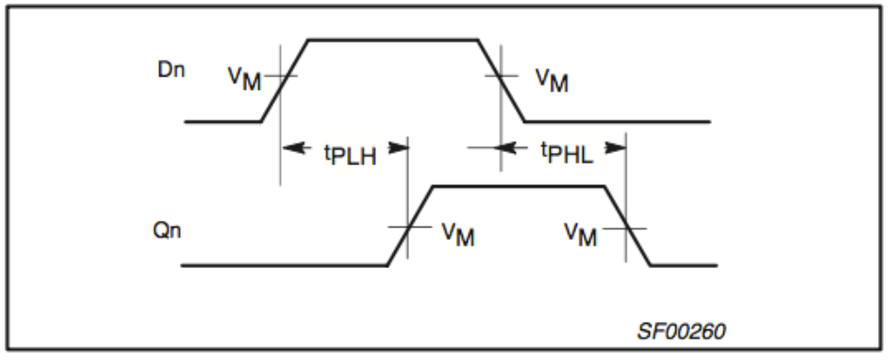
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25 °C, V_{CC} = +5.0 V, C_L = 50 pF, R_L = 500 Ω			T_{amb} = 0 °C to +70 °C, V_{CC} = +5.0 V ± 10%, C_L = 50 pF, R_L = 500 Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Set-up time, HIGH or LOW level Dn to E	74F373	Waveform 4	0 1.0			0 1.0		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW level Dn to E		Waveform 4	3.0 3.0			3.0 3.0		ns
t_w (H)	E Pulse width, HIGH		Waveform 1	3.5			4.0		ns
t_{su} (H) t_{su} (L)	Set-up time, HIGH or LOW level Dn to CP	74F374	Waveform 5	2.0 2.0			2.0 2.0		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW level Dn to CP		Waveform 5	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, HIGH or LOW		Waveform 5	3.5 4.0			3.5 4.0		ns



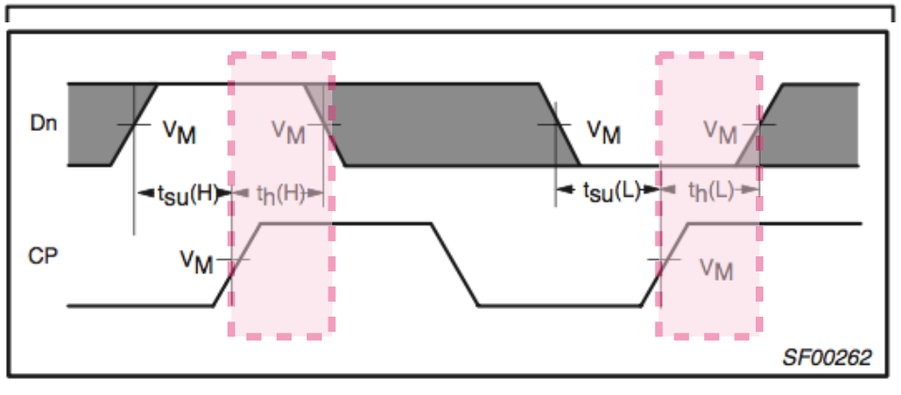
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency



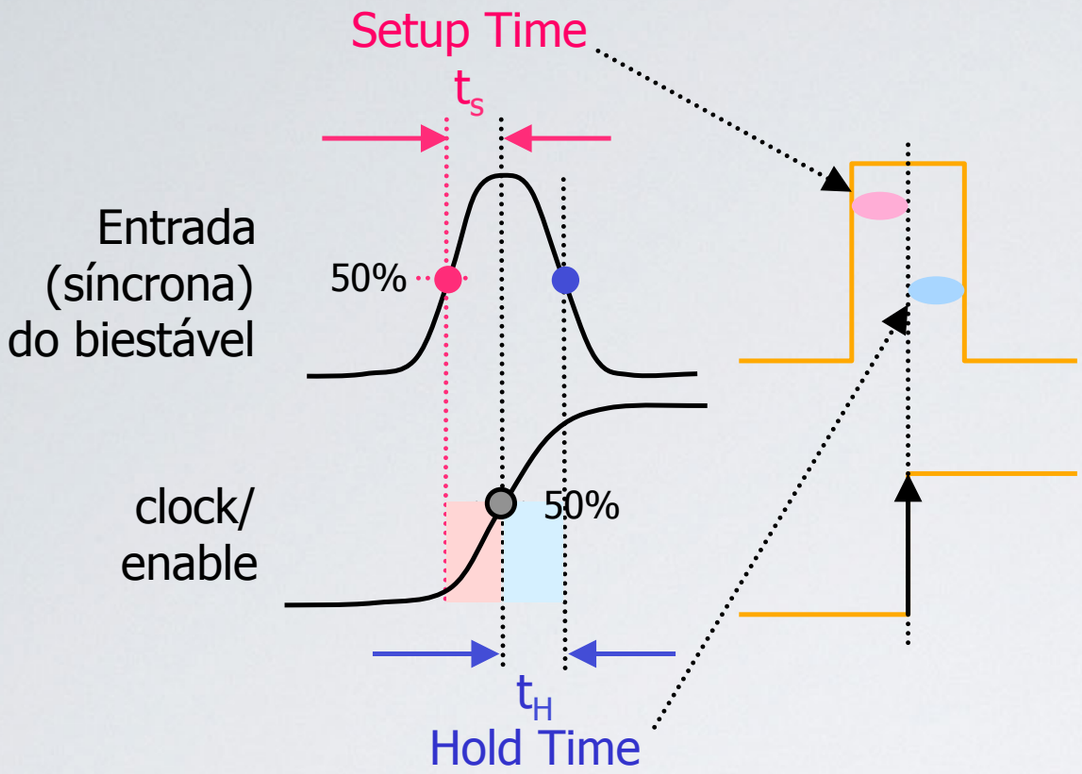
Waveform 2. Propagation delay for enable to output and enable pulse width

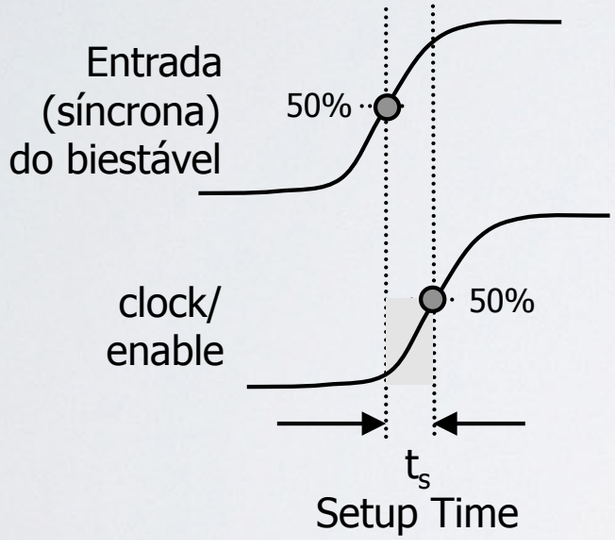


Waveform 3. Propagation delay for data to output



Waveform 5. Data set-up time and hold times

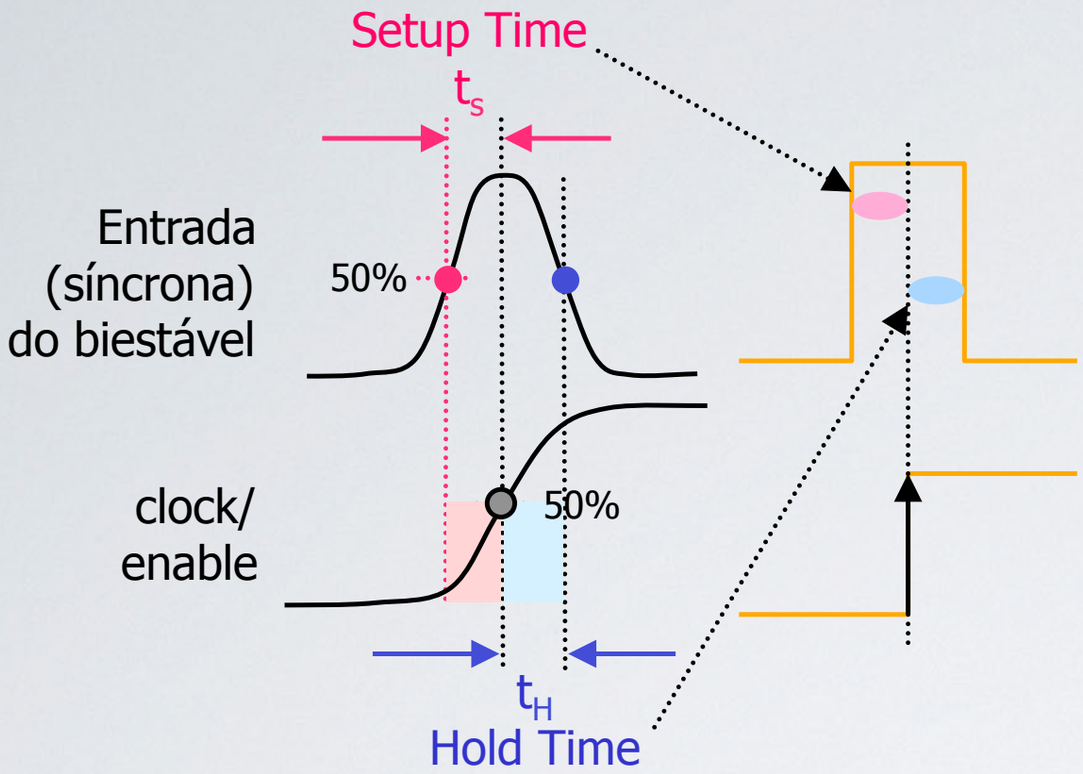


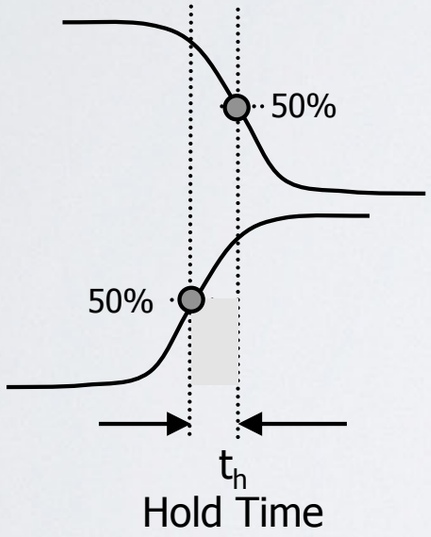


Setup Time (tempo de estabilização) – t_S:

É o intervalo de tempo mínimo durante o qual as entradas de um biestável não devem mudar ANTES da transição positiva (ou negativa) do sinal do clock (no caso dos Flip-Flops) ou ANTES da mudança de nível do sinal de enable (no caso dos Latches). Fabricante: t_s(min)

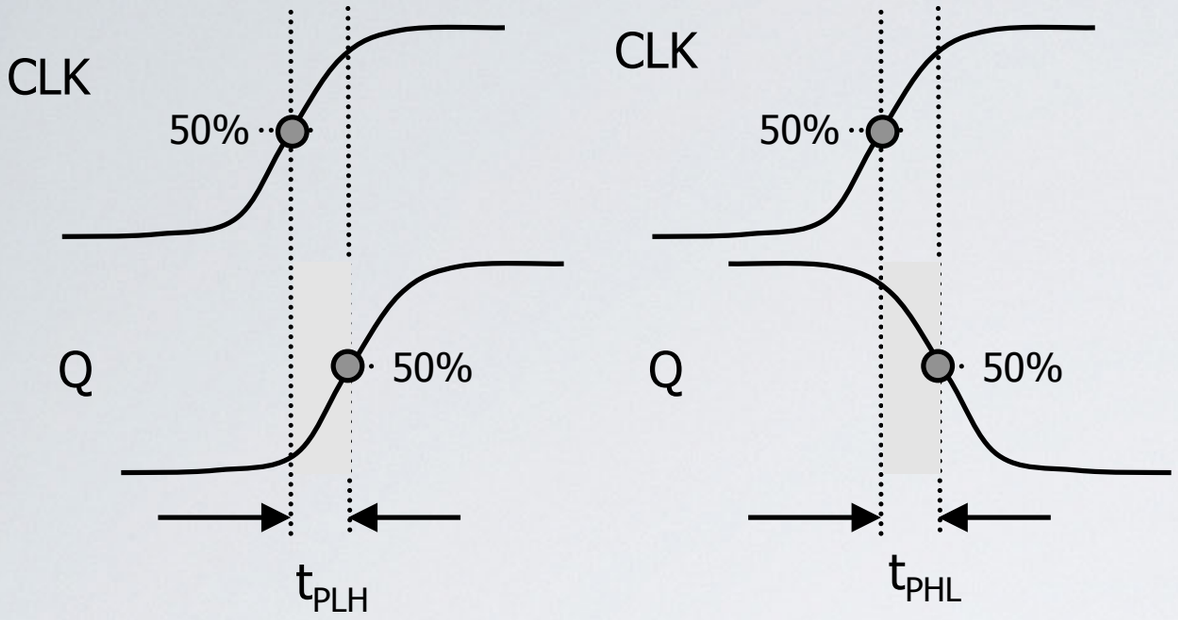
RESUMO CARACTERÍSTICAS "AC"





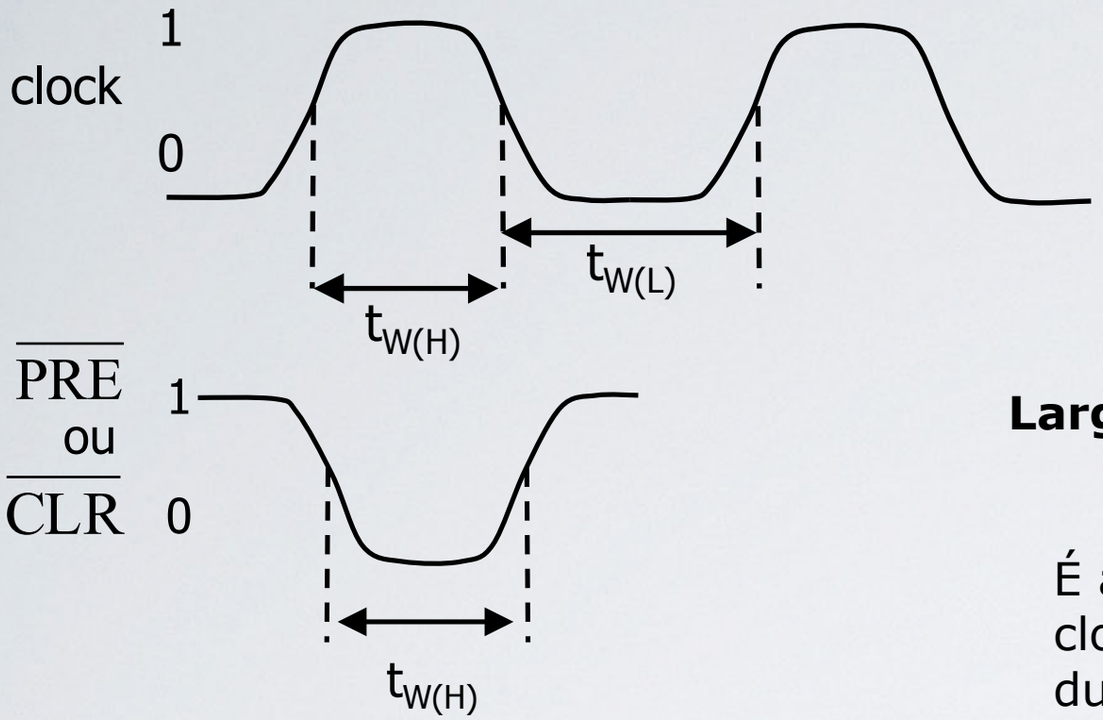
Hold Time (tempo de sustentação) – t_H:
É o intervalo de tempo mínimo durante o qual, as entradas de um biestável não devem mudar APÓS a transição do sinal do clock ou mudança de nível do sinal de enable. Fabricante: t_H(min)

RESUMO CARACTERÍSTICAS "AC"



Atrasos de Propagação (propagation delays) – t_{PLH}, t_{PHL}
São os atrasos que ocorrem nas saídas em resposta a transições nos sinais de entrada de um biestável.
Fabricantes: especificam os valores máximos: $t_{PLH(MAX)}$, $t_{PHL(MAX)}$ – Onde: t_{PLH} se refere ao atraso de propagação para comutação do nível lógico baixo (Low) para alto (High), normalmente na faixa de 10 à 100 ns.

RESUMO CARACTERÍSTICAS "AC"



Largura de Pulso – $t_{W(L)}$ e $t_{W(H)}$:

É a menor largura de pulso aceitável para a entrada de clock de um Flip-Flop, ou melhor, o menor tempo de duração em que o sinal de clock deve permanecer em nível lógico Baixo antes de ir para Alto ($t_{W(L)}$) e o tempo mínimo em que o sinal de clock deve ficar em nível lógico Alto antes de voltar para Baixo ($t_{W(H)}$). Estes tempos também se aplicam as entradas assíncronas de Preset/Set ou Clear/Reset. Normalmente da ordem de ns.

RESUMO CARACTERÍSTICAS "AC"

		TTL			CMOS	
		7474	74LS112		74C74	74HC112
t_S		20	20		60	25
t_H		5	0		0	0
t_{PHL}	de CLK para Q	40	24		200	31
t_{PLH}	de CLK para Q	25	16		200	31
t_{PHL}	de $\overline{CLR}$ para Q	40	24		225	41
t_{PLH}	de $\overline{PRE}$ para Q	25	16		225	41
$t_{W(L)}$	CLK LOW time	37	15		100	25
$t_{W(H)}$	CLK HIGH time	30	20		100	25
$t_{W(L)}$	para $\overline{CLR}$ ou $\overline{PRE}$	30	15		60	25
f_{MAX}	(MHz)	15	30		5	20

Obs:
- 7474 = duplo FF-D (TTL padrão)
- 74LS112 = duplo FF-JK (low-power Schottky TTL)
- 74C74 = duplo FF-D (CMOS padrão)
- 74HC122 = duplo FF-JK (high speed CMOS)

RESUMO CARACTERÍSTICAS "AC"

A Figura 5.12 mostra um circuito simples que pode ser usado para detectar a interrupção de um feixe de luz. A luz é focalizada em um fototransistor conectado em uma configuração emissor-comum para operar como uma chave. Considere que o latch tenha sido previamente levado para o estado 0 (resetado) ao abrir a chave SW1 momentaneamente e descreva o que acontece se o feixe de luz for momentaneamente interrompido.

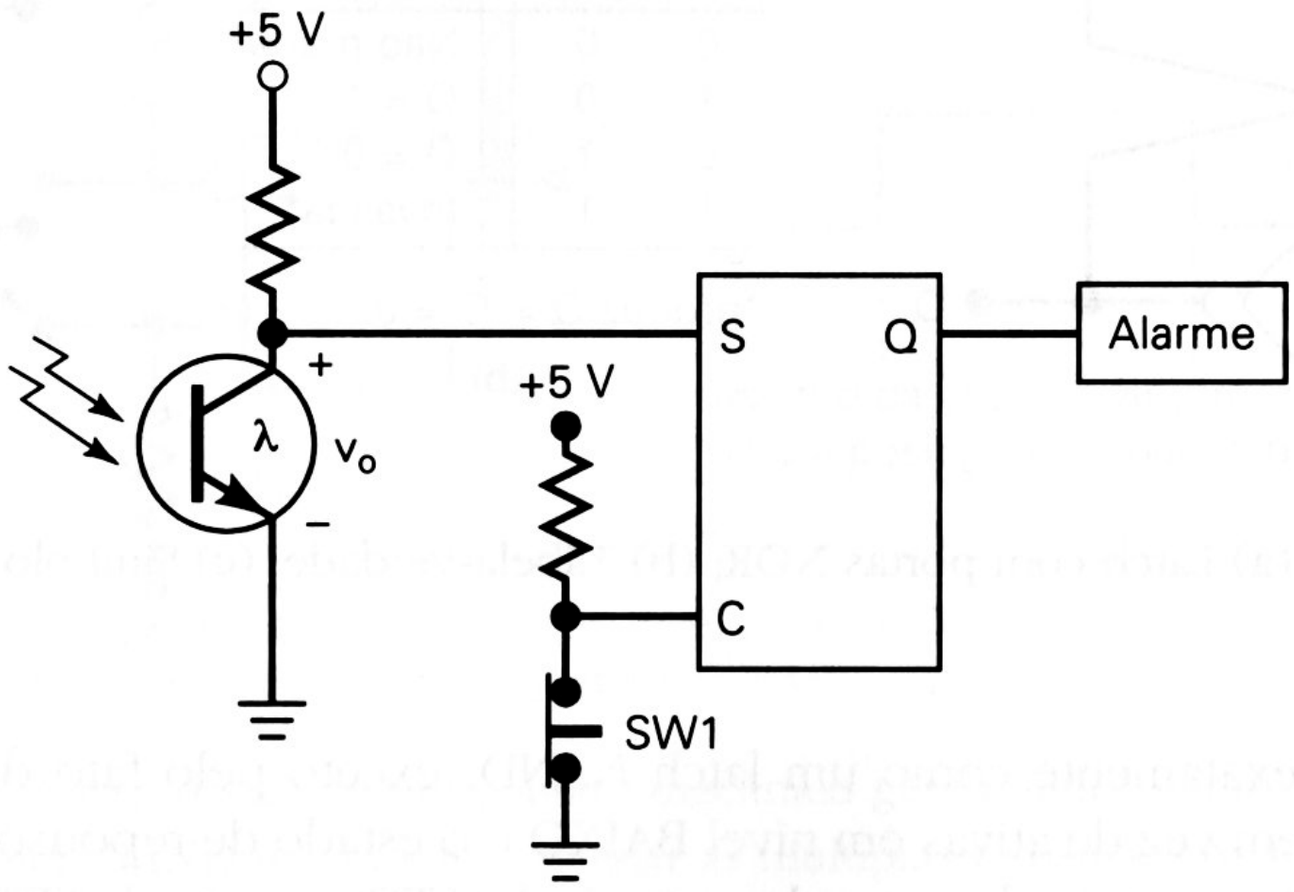
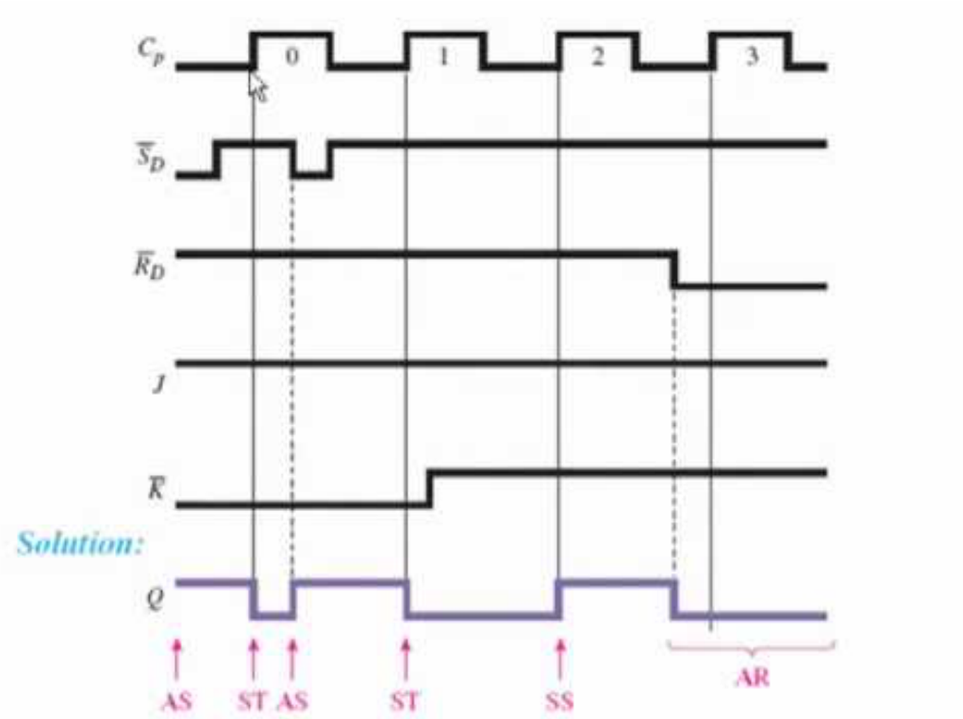
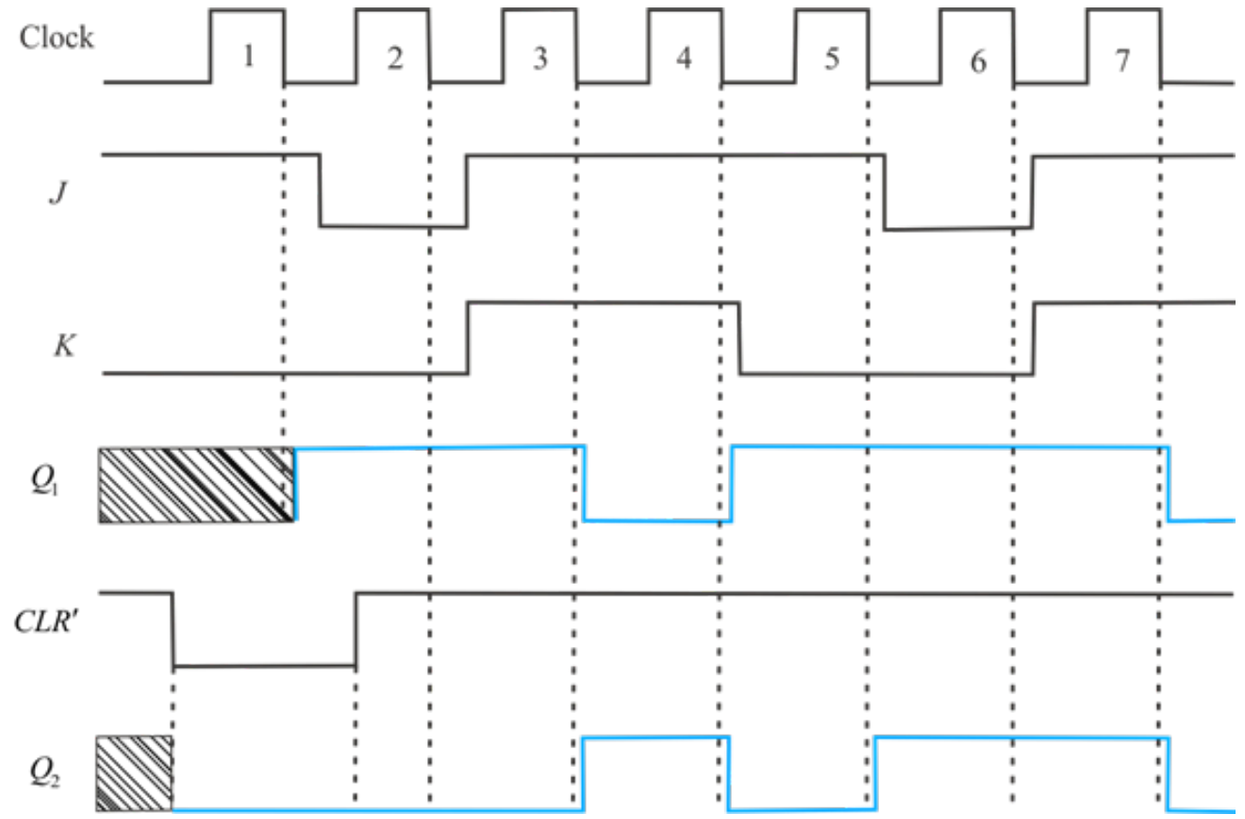


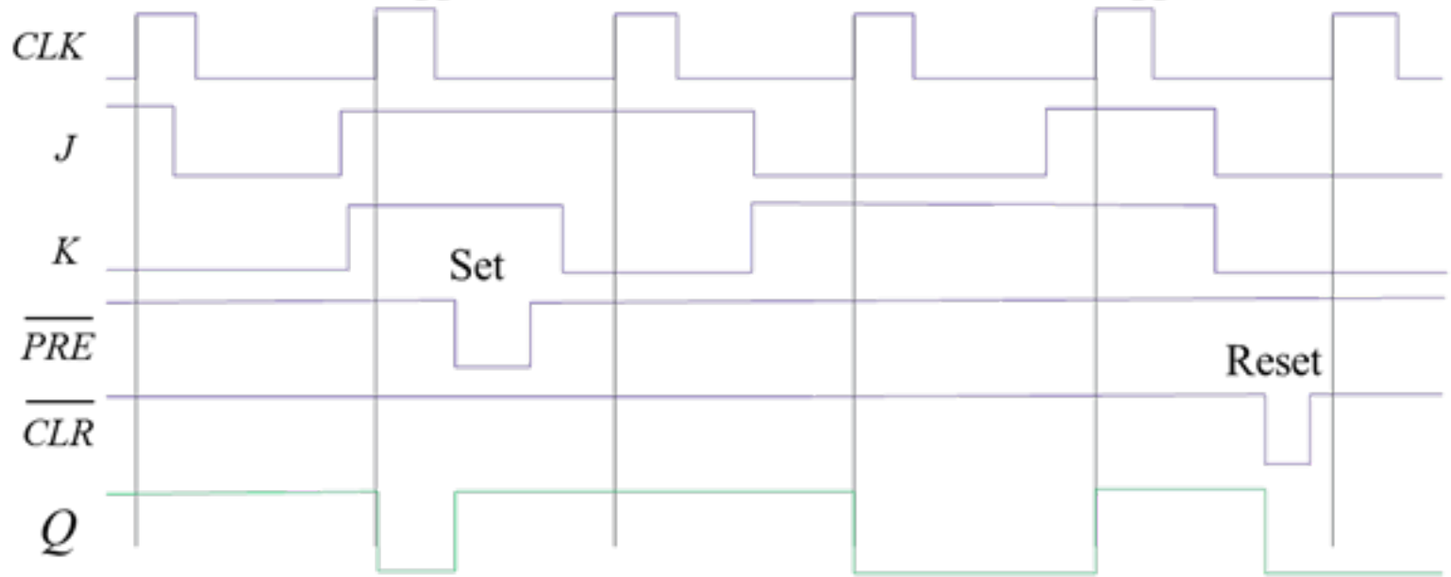
FIGURA 5.12 Exemplo 5-4.

APLICAÇÃO

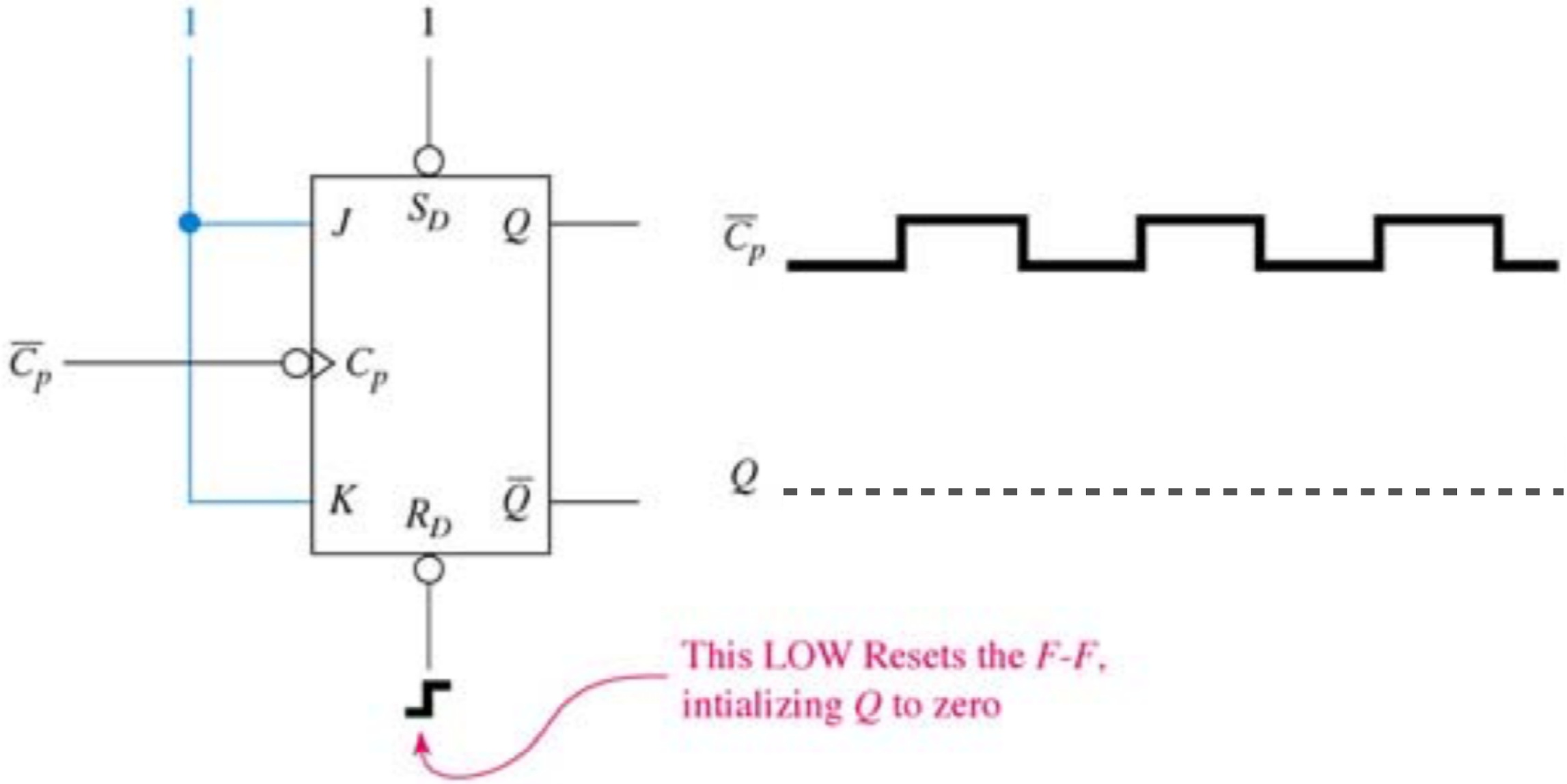




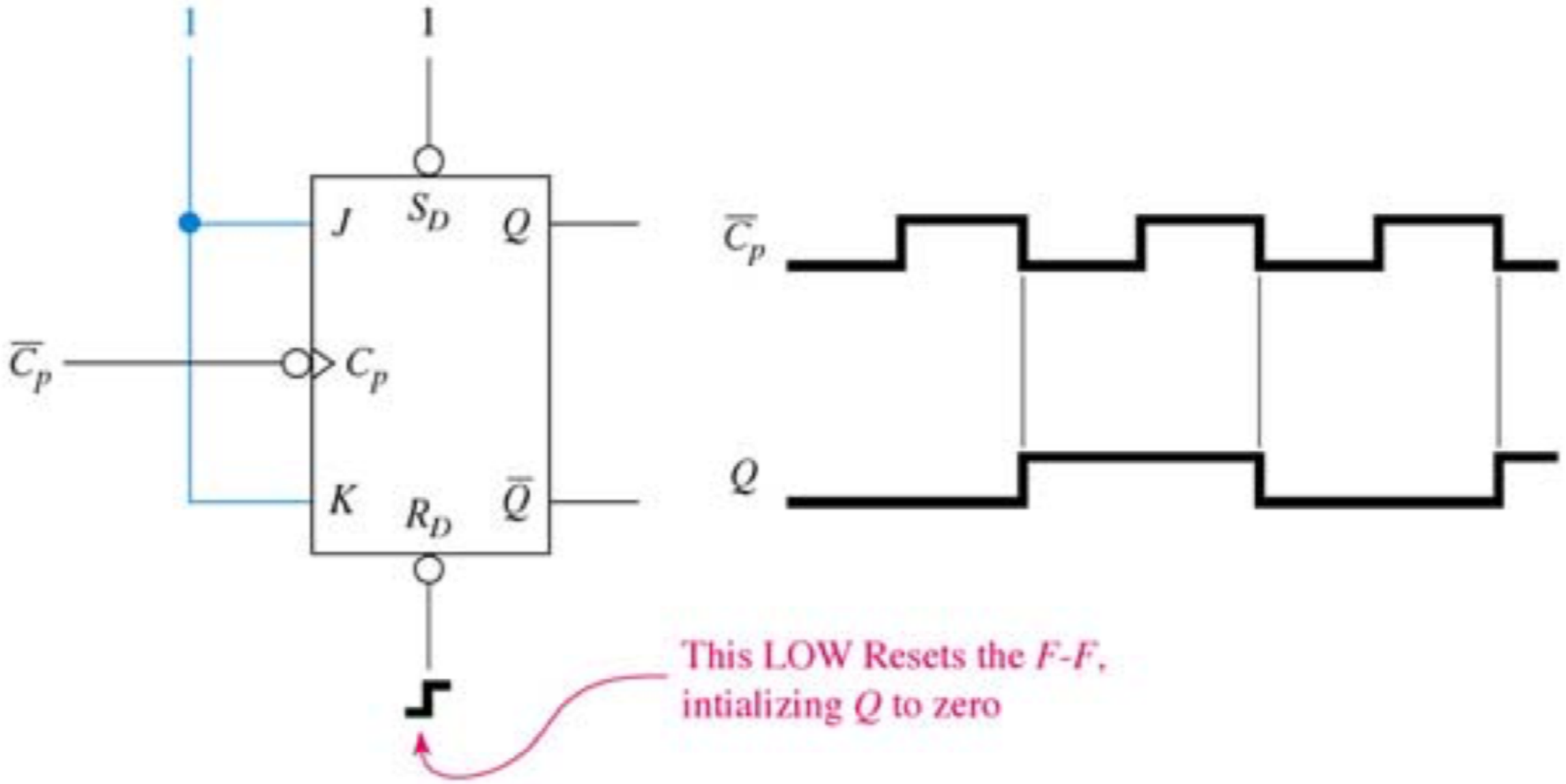
Set Toggle Set Reset Toggle Latch



EXERCÍCIOS

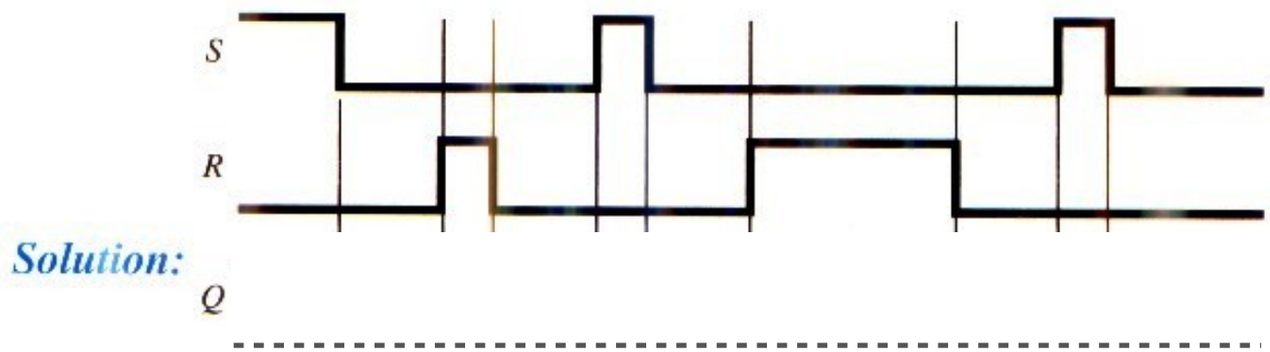


OPERAÇÃO TOGGLE



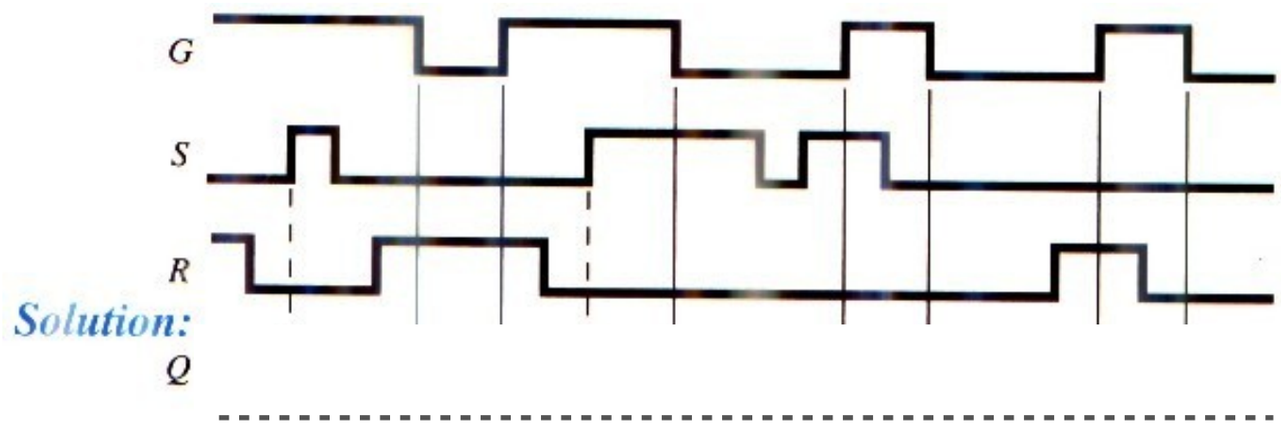
OPERAÇÃO TOGGLE

Complete as formas de onda:

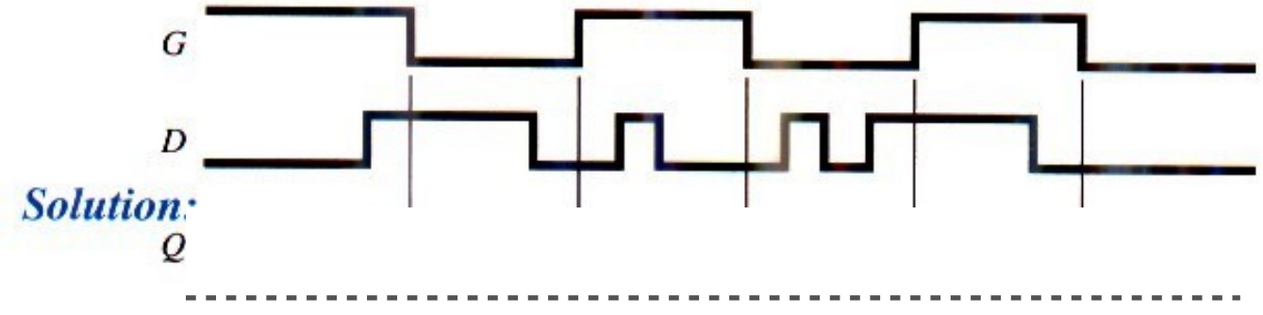


← Biestável RS

Function

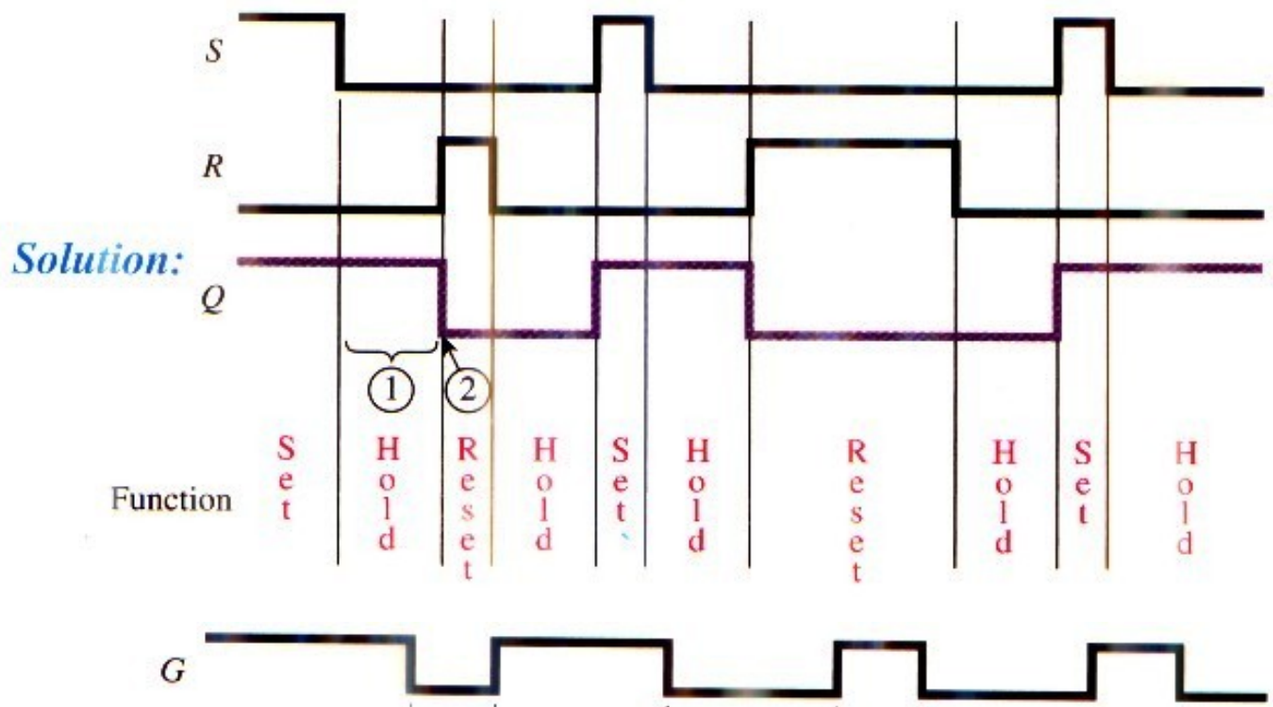


← Latch RS

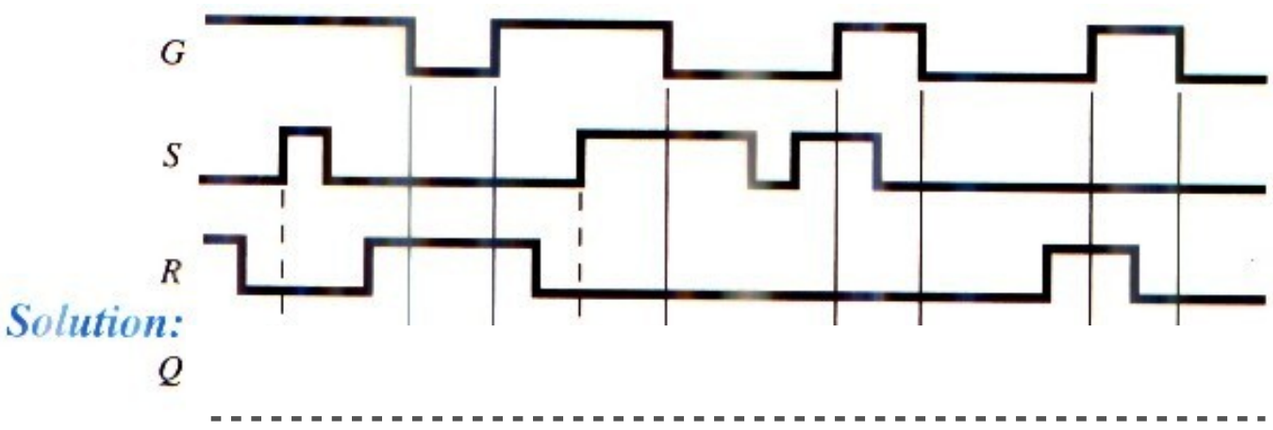


← Latch D

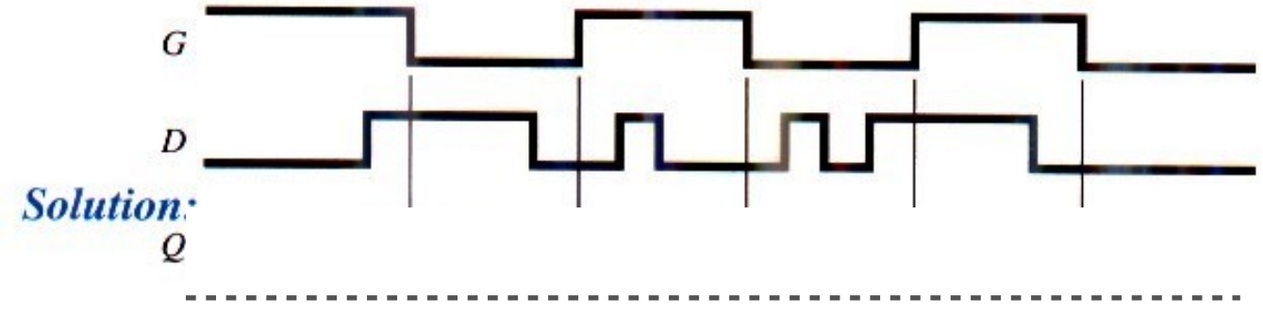
Complete as formas de onda:



← Biestável RS

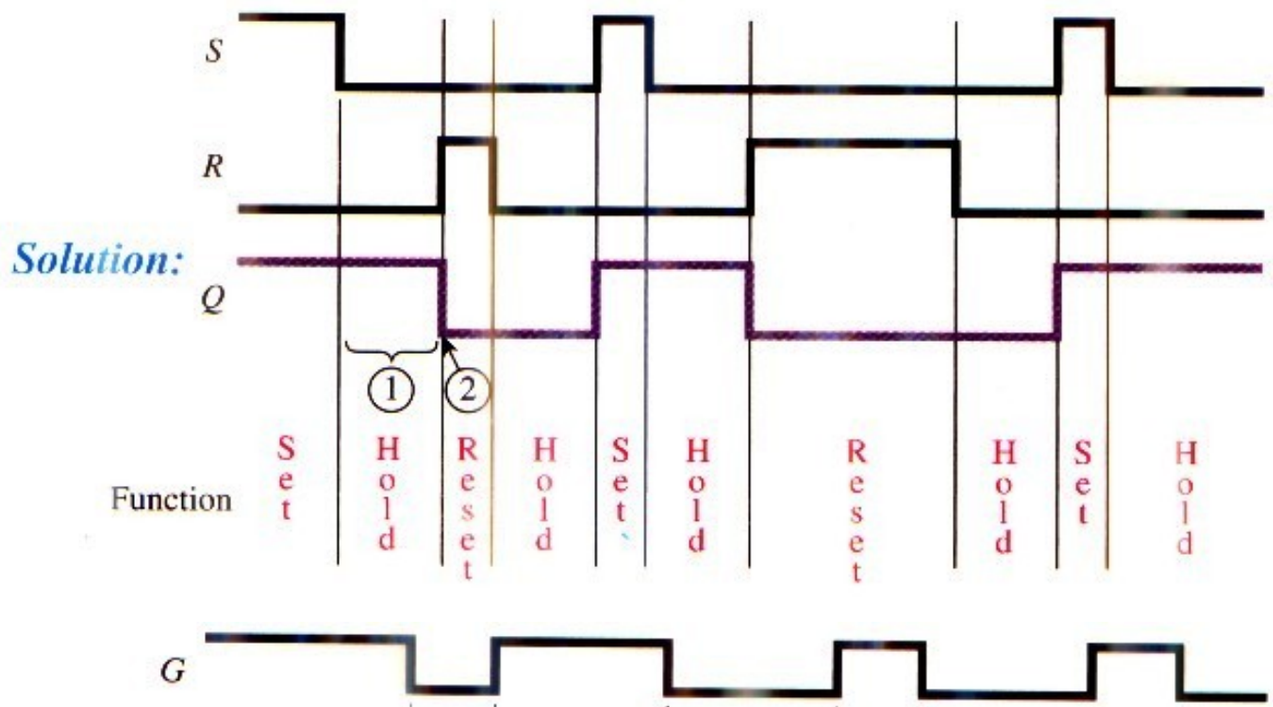


← Latch RS

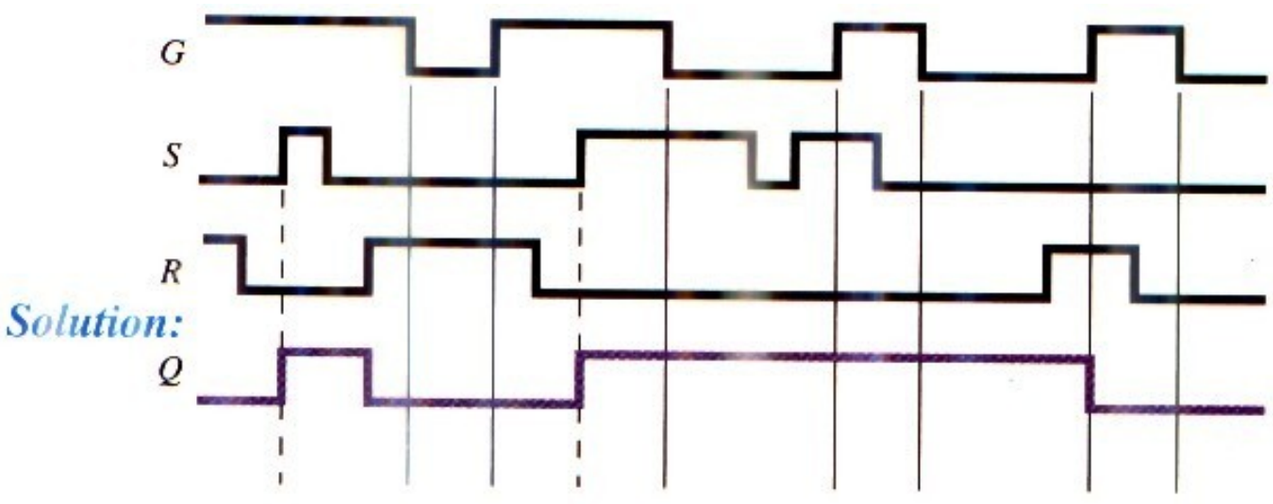


← Latch D

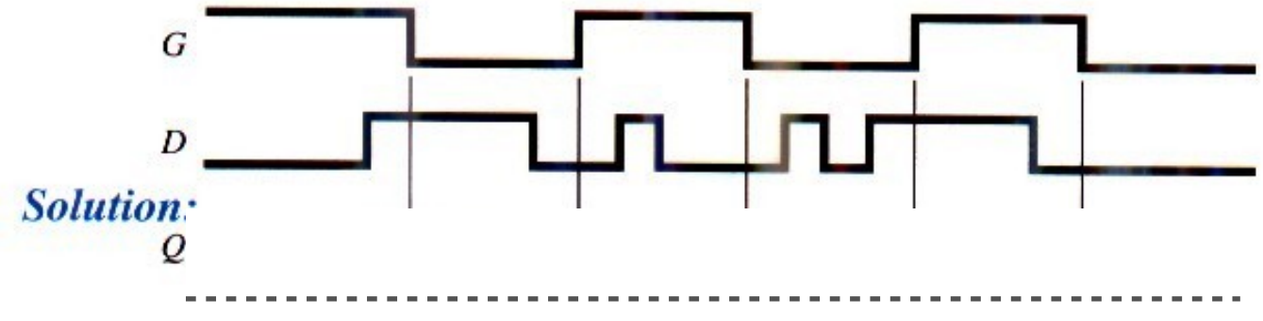
Complete as formas de onda:



⬅ Biestável RS

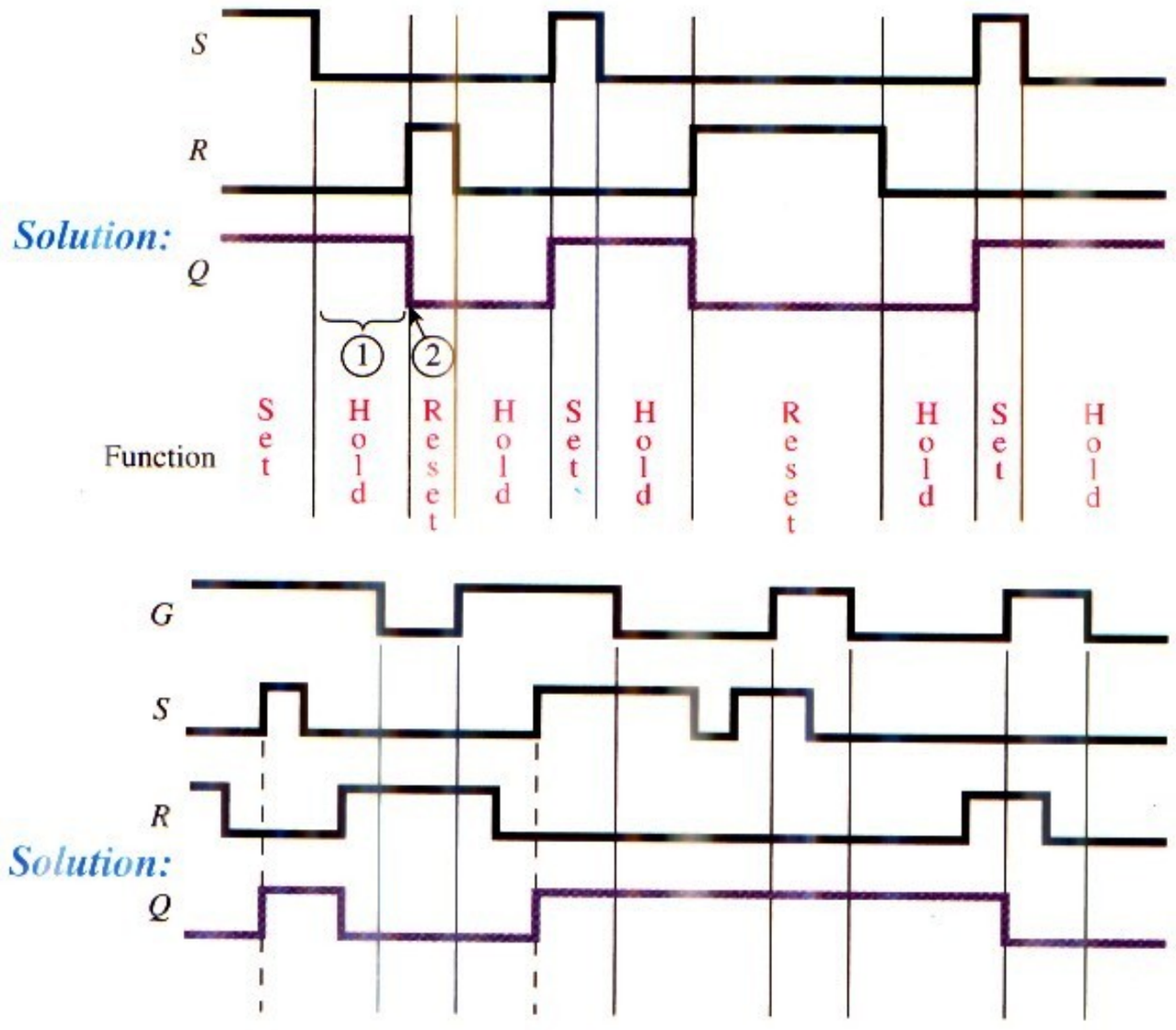


⬅ Latch RS



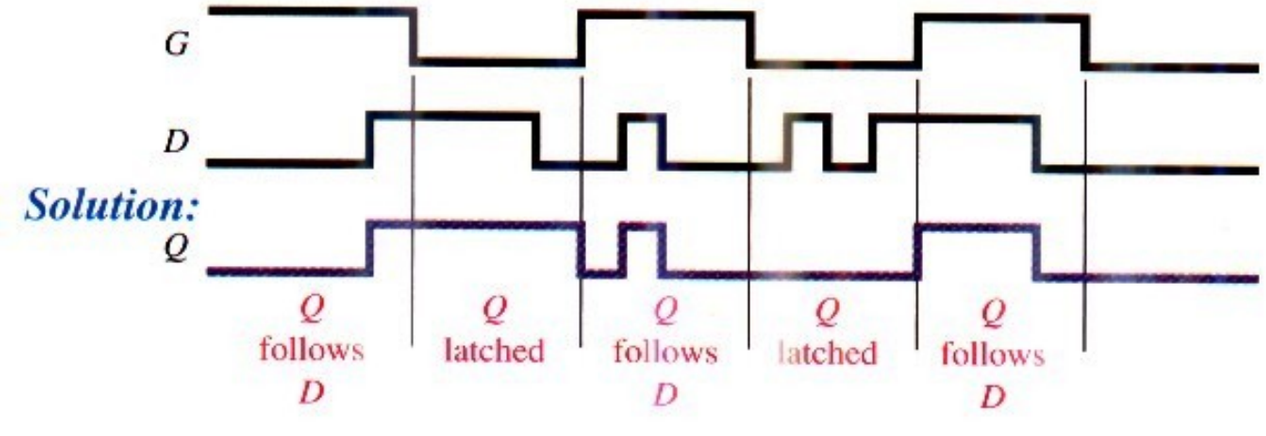
⬅ Latch D

Complete as formas de onda:



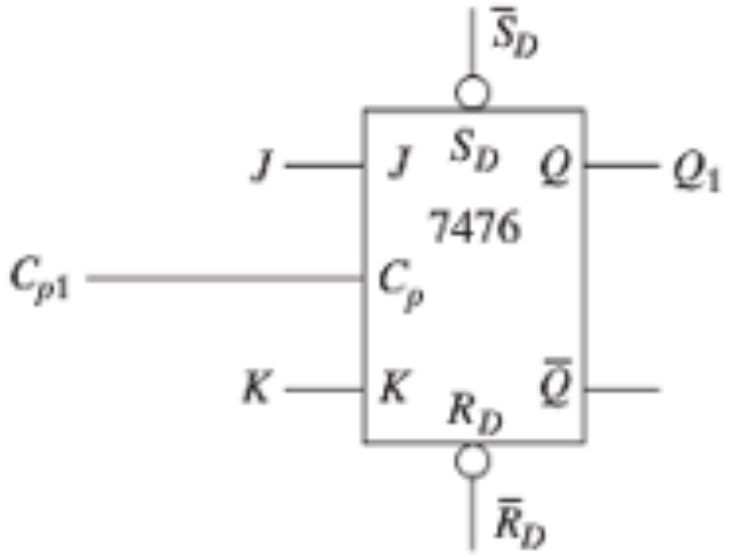
⬅ Biestável RS

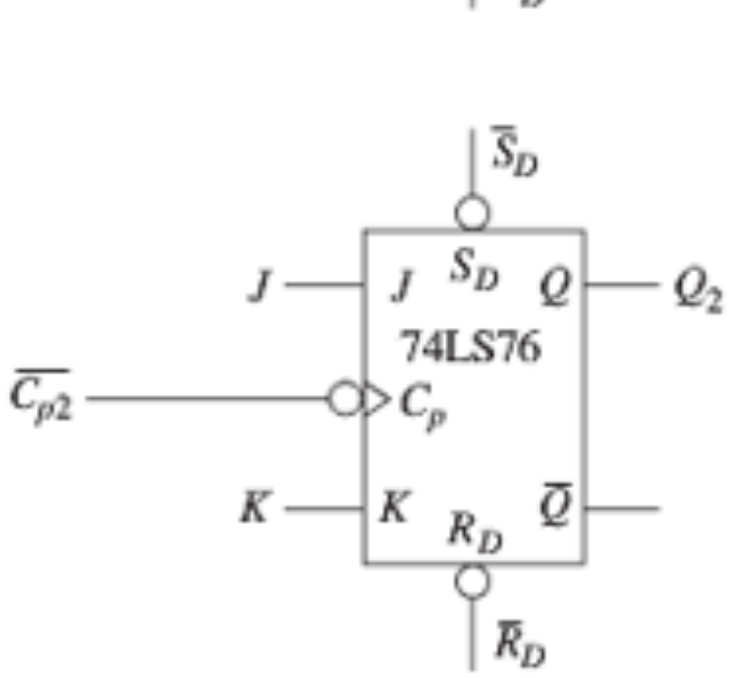
⬅ Latch RS

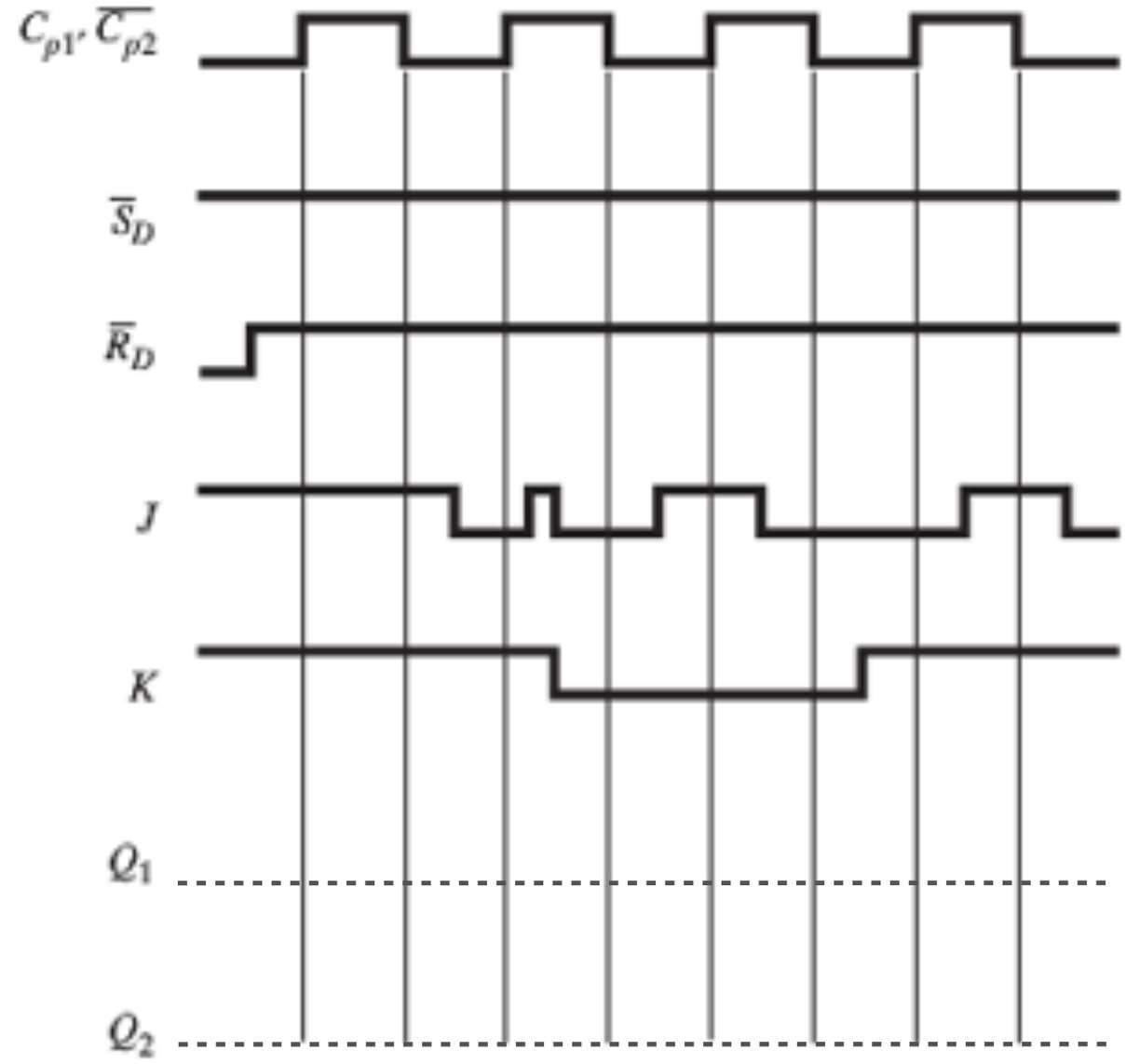


⬅ Latch D

The logic symbol and input waveforms for both the 7476 and 74LS76 are given in Figure P10–26. Sketch the waveform at each Q output.



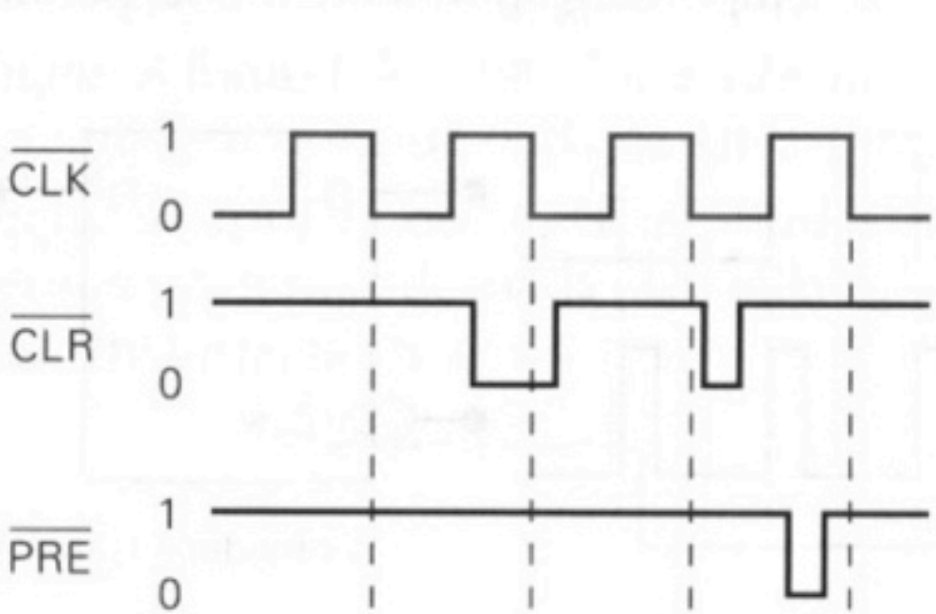




Complete as formas de onda para os dois FFs acima.

(Note que o primeiro é ativado por borda de subida e o segundo por borda de descida).

5-20. Determine a forma de onda da saída Q do FF mostrado na Figura 5.69. Considere inicialmente $Q = 0$ e lembre-se de que as entradas assíncronas se sobrepõem a todas as outras entradas.



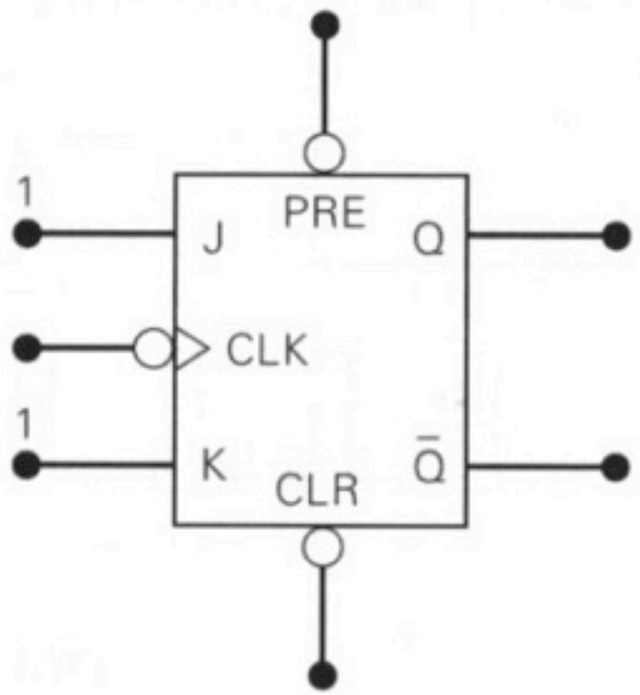


FIGURA 5.69 Problema 5-20.

5-12. As formas de onda mostradas na Figura 5.65 são aplicadas em dois FFs diferentes:

(a) *J-K* disparado por borda positiva

(b) *J-K* disparado por borda negativa

Desenhe a forma de onda da saída Q para cada um desses FFs, considerando inicialmente $Q = 0$. Considere que cada FF tenha t_H e $t_s > 0$.

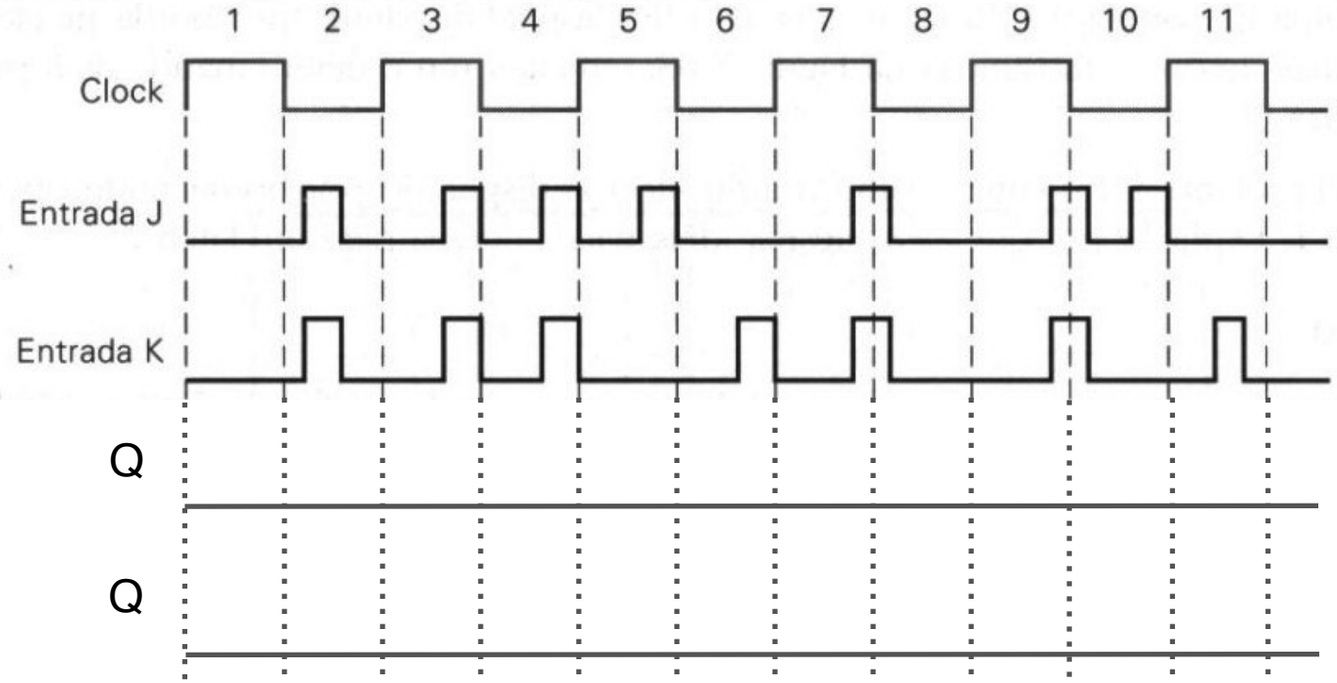


FIGURA 5.65 Problema 5-12.

← JK ↑

← JK ↓

5-18. Compare a operação do latch *D* com o flip-flop *D* disparado por borda negativa aplicando as formas de onda, mostradas na Figura 5.68, em cada um e determinando as formas de onda das saídas *Q*.

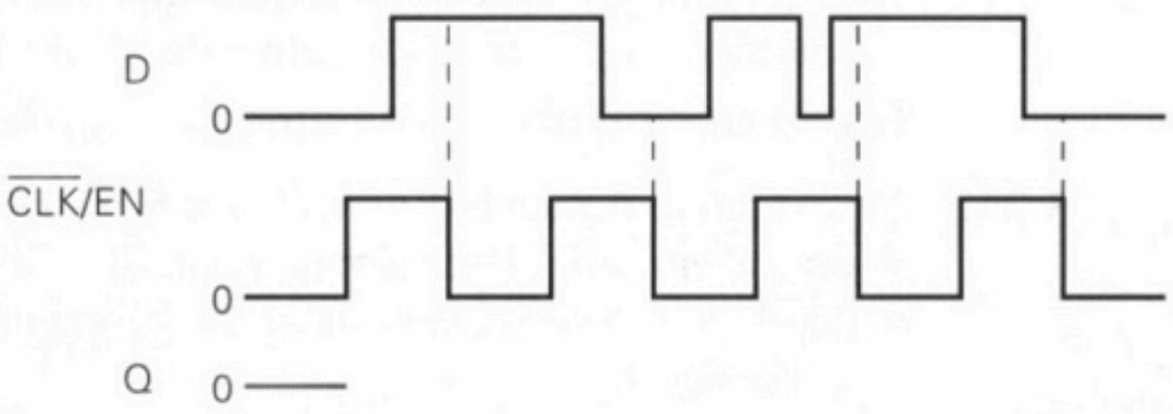


FIGURA 5.68 Problema 5-18.

N 5-13. Um FF *D* algumas vezes é usado para *atrasar* uma forma de onda binária de forma que a informação binária aparece na saída um certo tempo depois de aparecer na entrada *D*.

(a) Determine a forma de onda da saída *Q* do FF mostrado na Figura 5.66 e compare com a forma de onda da entrada. Observe que o atraso de tempo em relação à entrada é de um período do clock.

(b) Como pode ser obtido um atraso de tempo correspondente a dois períodos do clock?

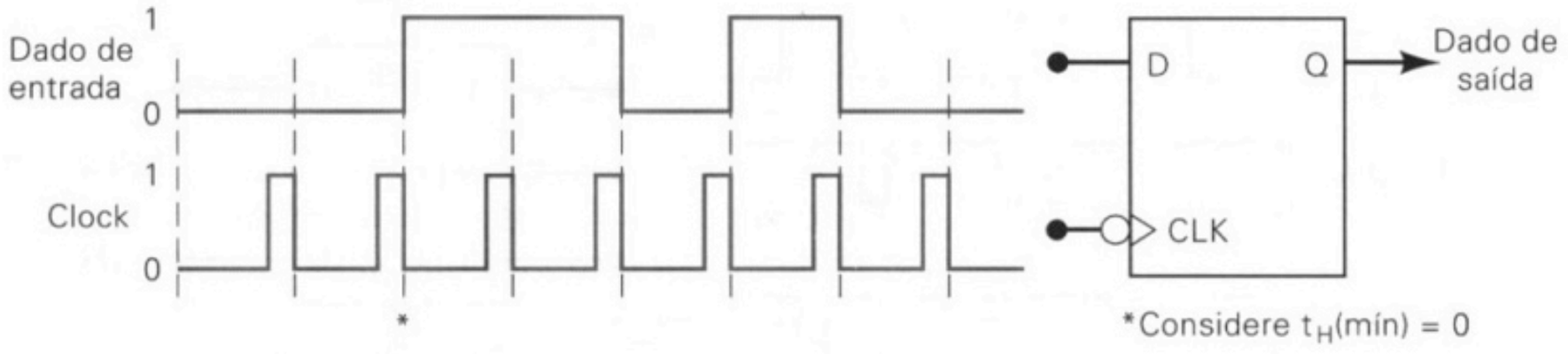


FIGURA 5.66 Problema 5-13.

5-15. Um FF *D* disparado por borda pode ser configurado para operar como um FF tipo T conforme é mostrado na Figura 5.67. Considere inicialmente $Q = 0$ e determine a forma de onda da saída *Q*.

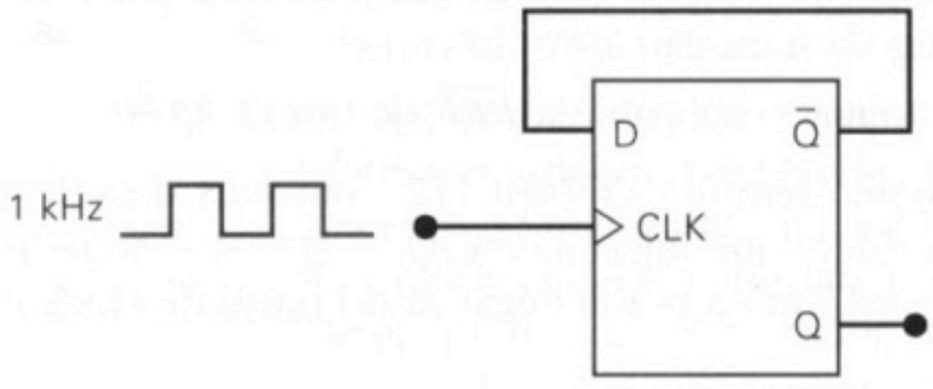
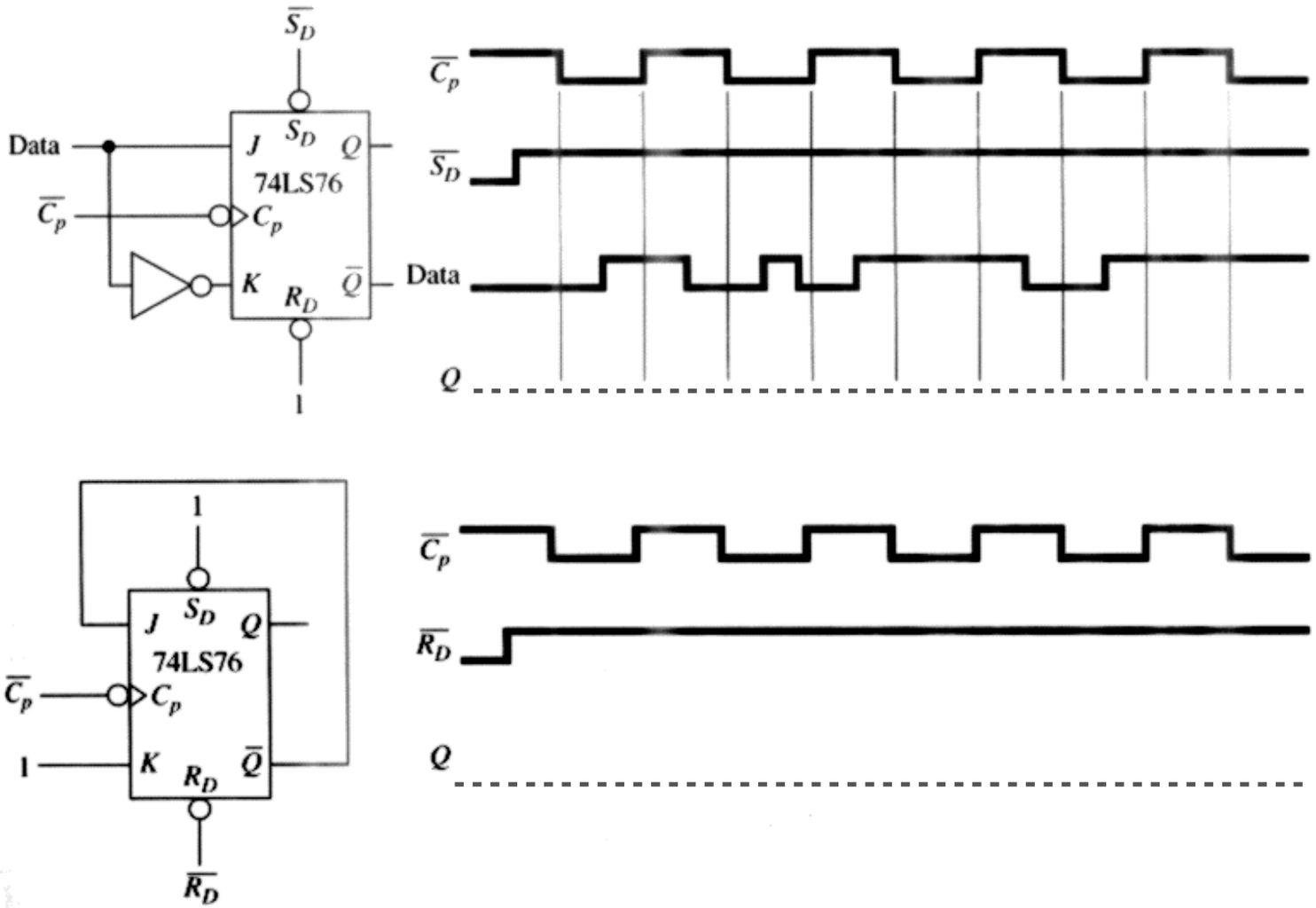


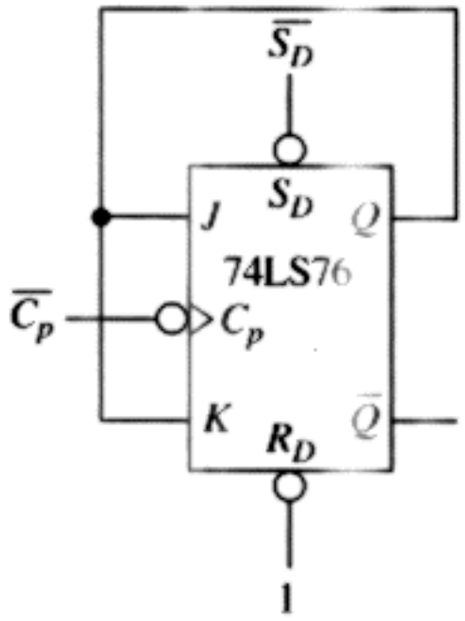
FIGURA 5.67 Flip-flop D configurado como um FF tipo T (Problemas 5-15 e 5-16).

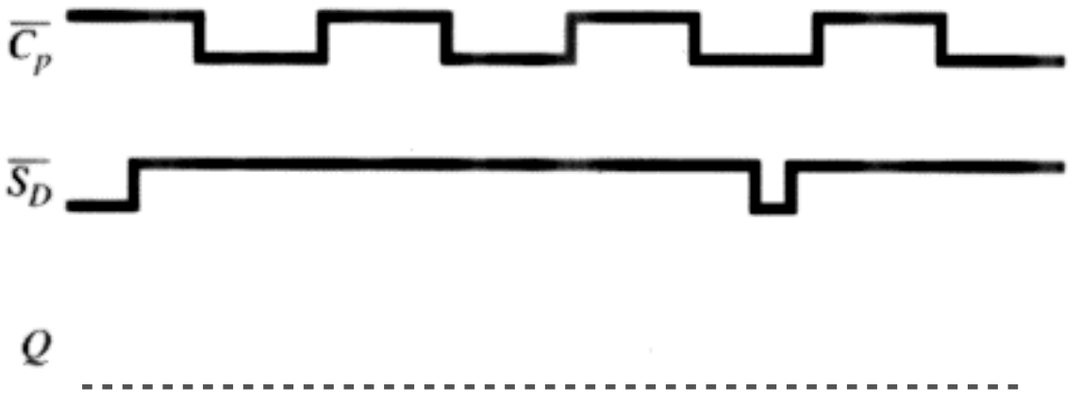
5-16. Altere o circuito mostrado na Figura 5.67 de forma que a saída *Q* seja conectada na entrada *D*. Em seguida, determine a forma de onda da saída *Q*.

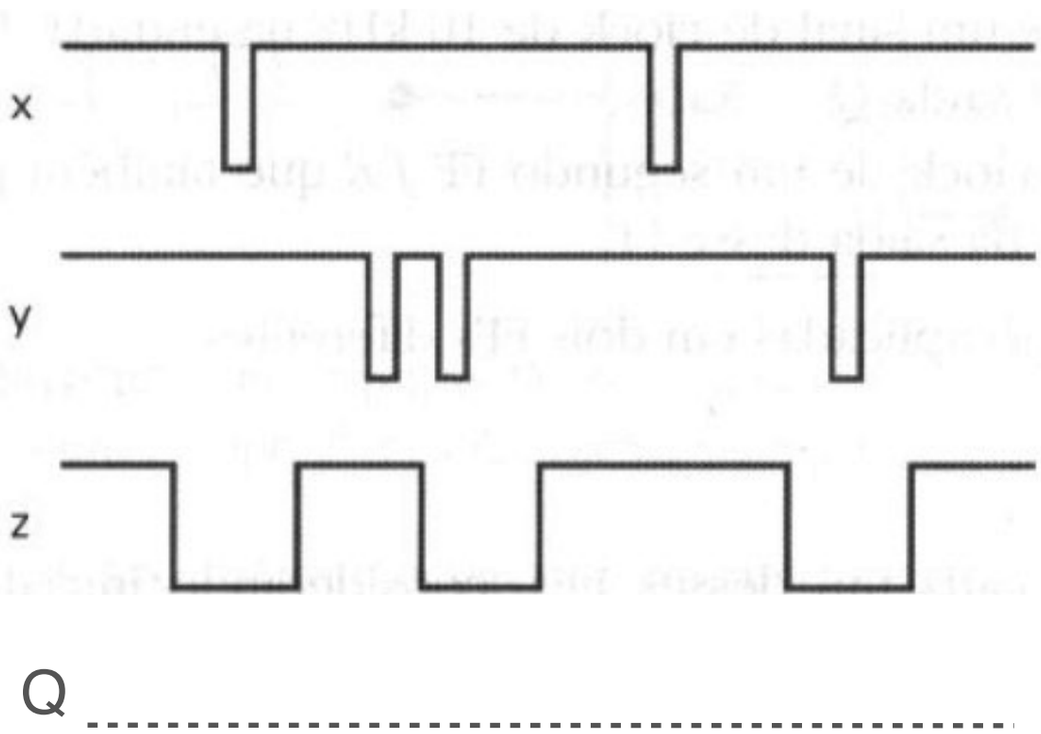
Complete as formas de onda:



Complete as formas de onda:







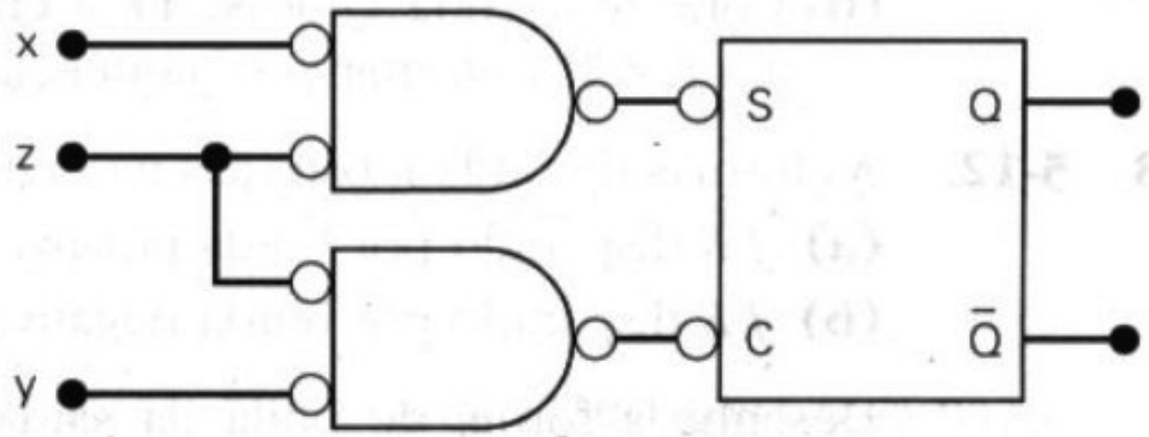


FIGURA 5.62 Problema 5.3.

ra 5.61 são aplicadas ao circuito da Figura 5.62. Considere
na de onda da saída *Q*.

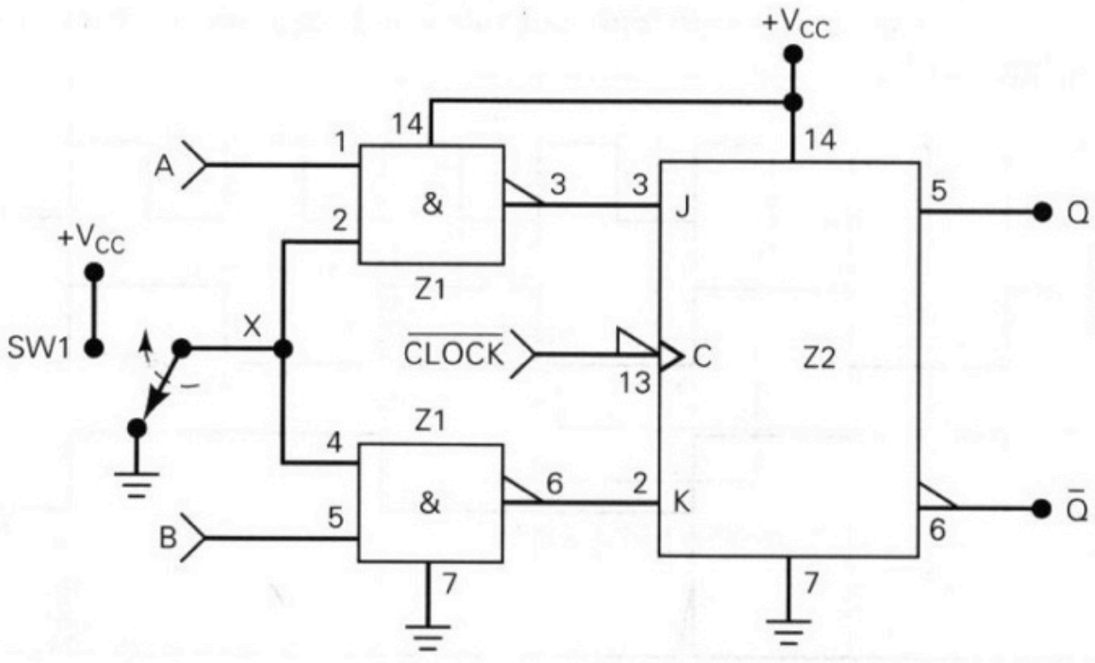
5-54. Veja o circuito mostrado na Figura 5.77. Considere que os CIs sejam todos da família lógica TTL. A forma de onda da saída Q foi obtida quando o circuito foi testado com os sinais de entrada mostrados e com a chave na posição voltada para cima; Essa forma de onda não está correta. Considere a seguinte lista de defeitos, e para cada uma indique "sim" ou "não" caso o defeito em questão possa ser a causa do defeito real. Justifique cada resposta.

(a) O ponto X está sempre em nível BAIXO em virtude de um defeito na chave.

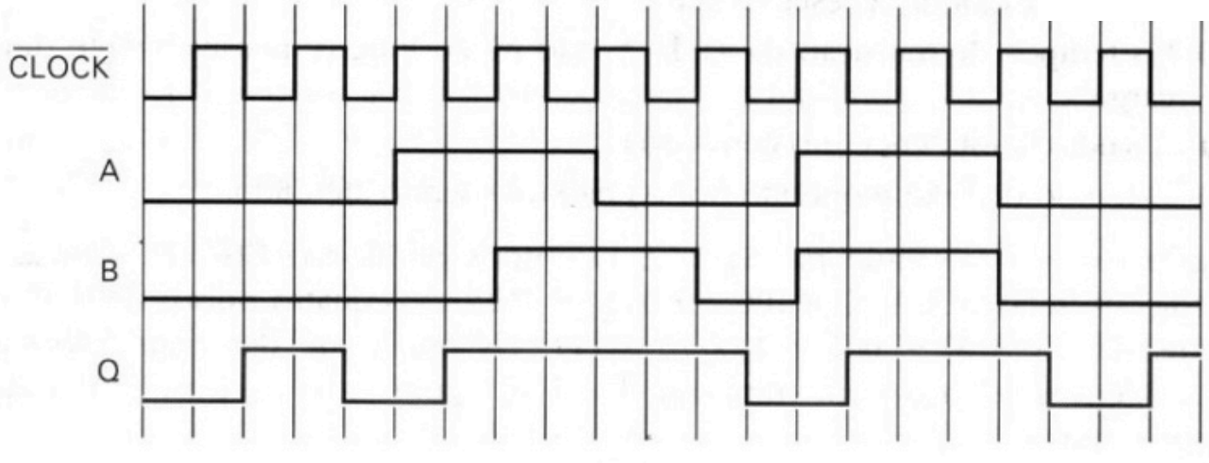
(b) O pino 1 de Z1 está internamente em curto com V_{CC}.

(c) A conexão entre Z1-3 e Z2-3 está aberta.

(d) Existe uma ponte de solda entre os pinos 6 e 7 de Z1.



(a)

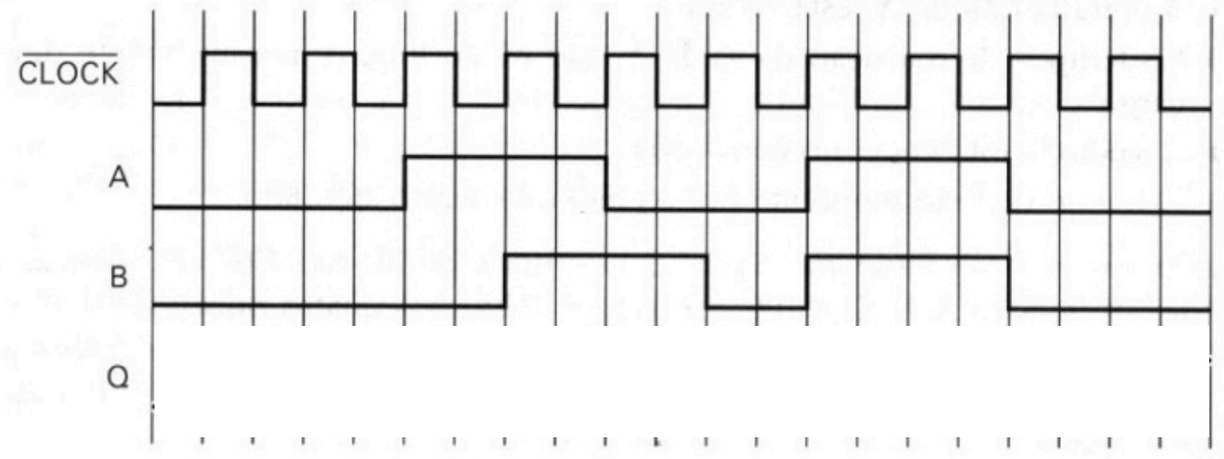


(b)

FIGURA 5.77 Problema 5-54.

Z1: 74LS00
Z2: 74LS114A

Correção:



Forma de onda esperada.

5-26. No circuito mostrado na Figura 5.71, as entradas *A*, *B* e *C* estão inicialmente em nível BAIXO. Supõe-se que a saída *Y* vá para o nível ALTO apenas quando *A*, *B* e *C* forem para o nível ALTO em uma determinada seqüência.

(a) Determine a seqüência que faz com que *Y* vá para nível ALTO.

(b) Explique a necessidade do pulso START.

(c) Modifique esse circuito de forma a usar FFs *D*.

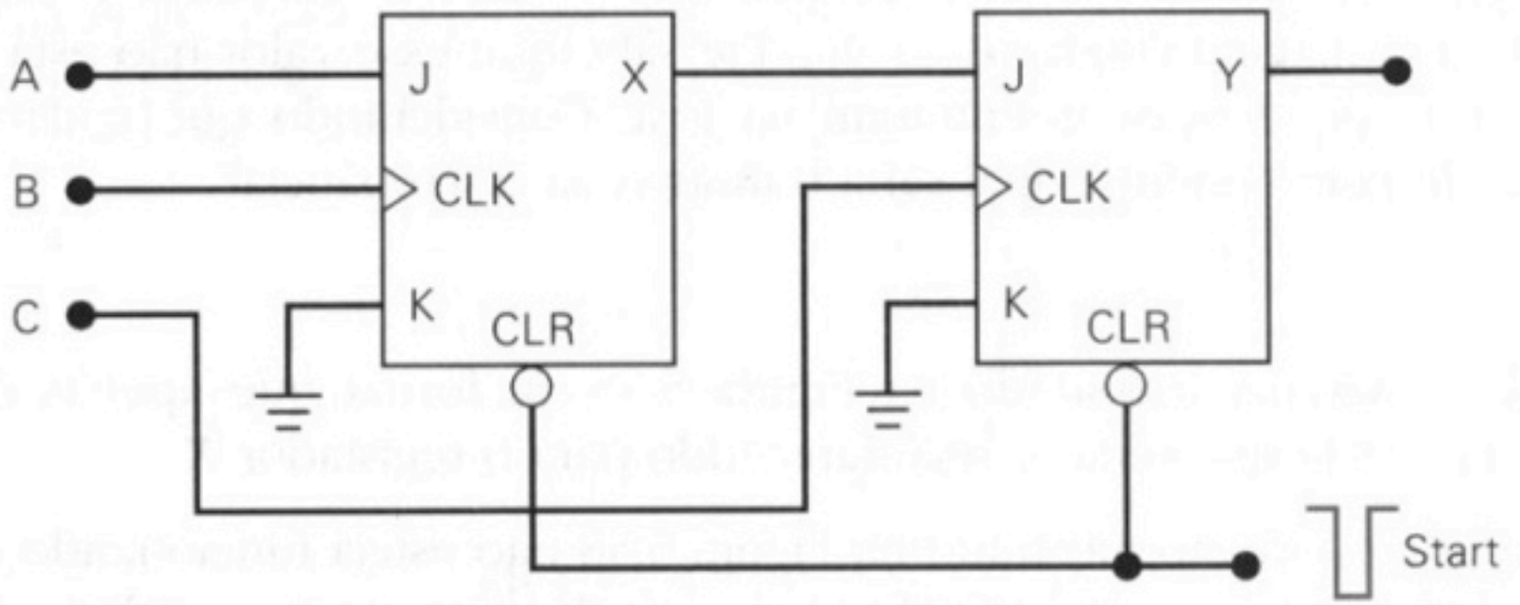
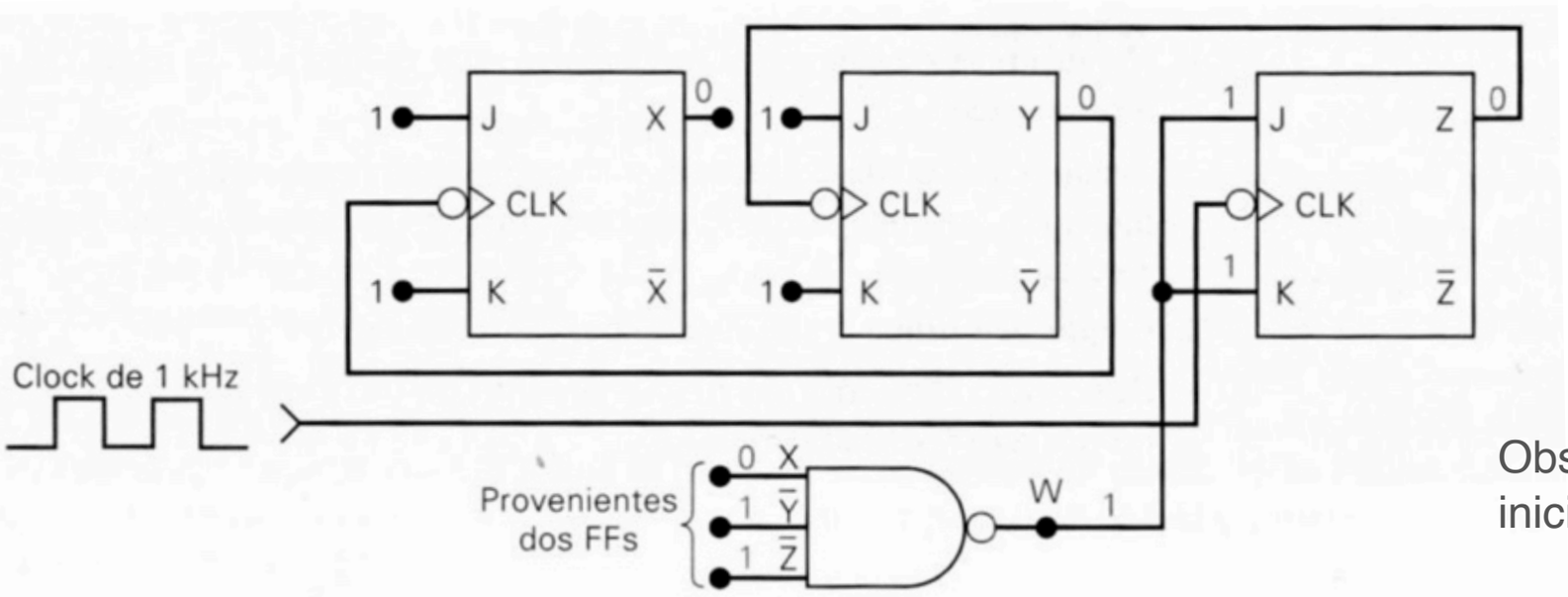
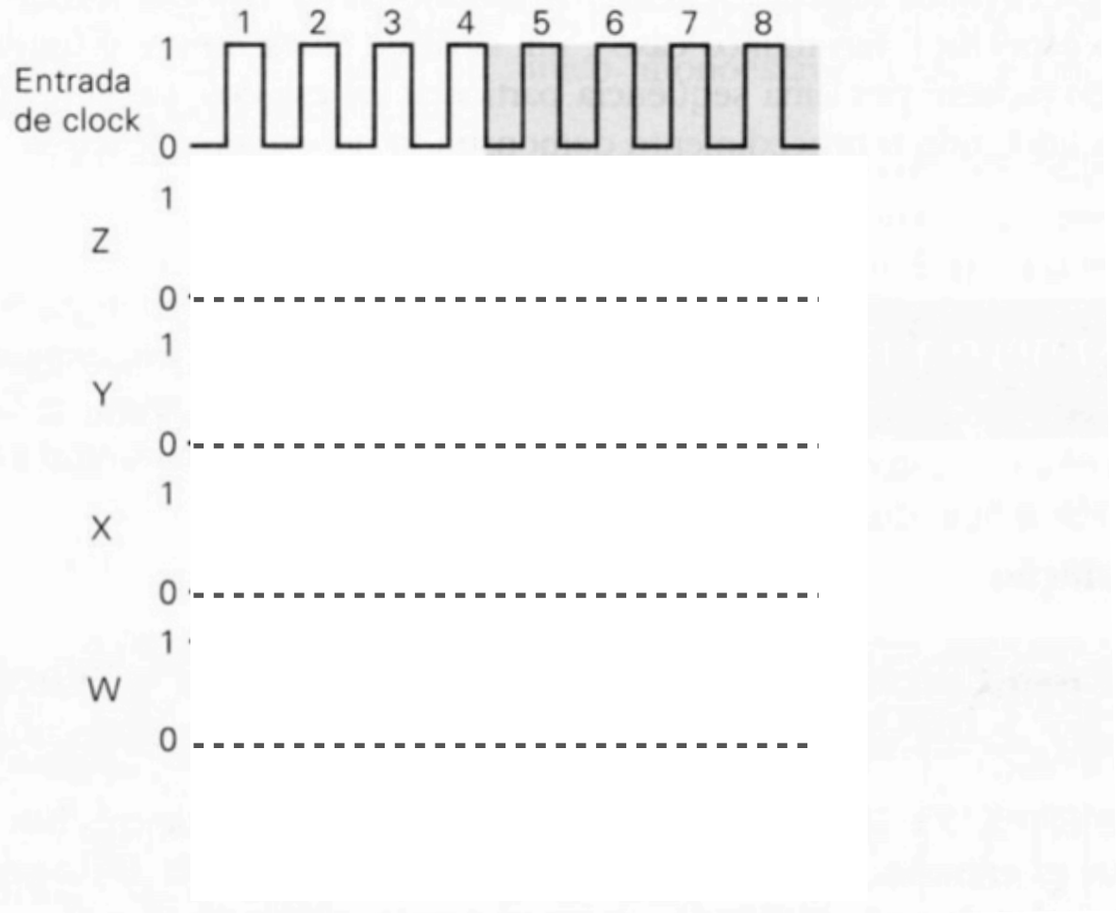


FIGURA 5.71 Problema 5-26.

Complete as formas de onda:





Obs.: Considere que todos os FF's iniciam resetados.