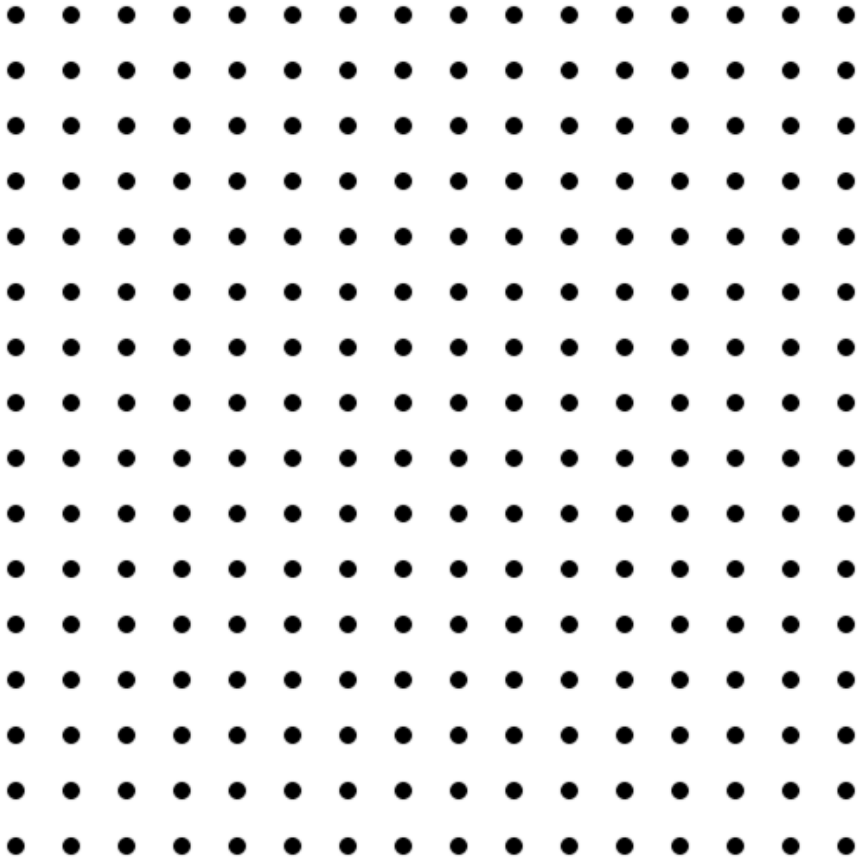


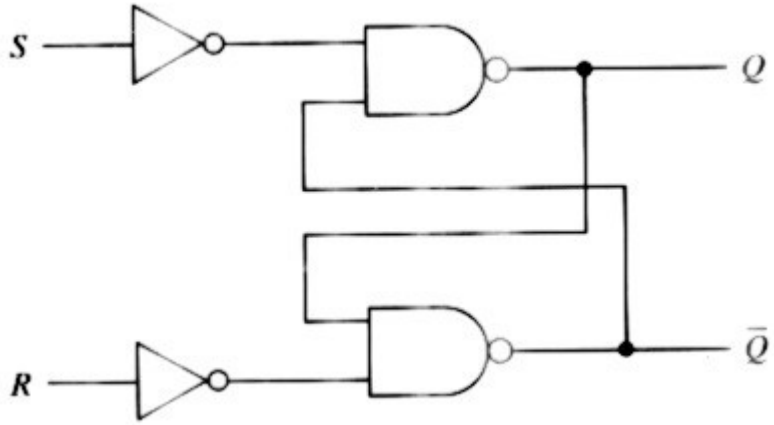
Biestáveis

Circuitos Digitais II

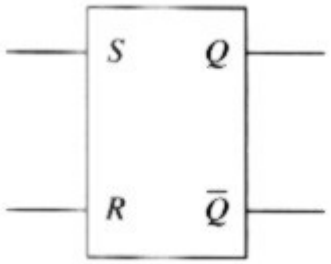
Prof. Fernando Passold

Biestáveis

Biestável RS básico:



a) Circuito interno com portas NOT e NAND.



b) Símbolo do Biestável RS.

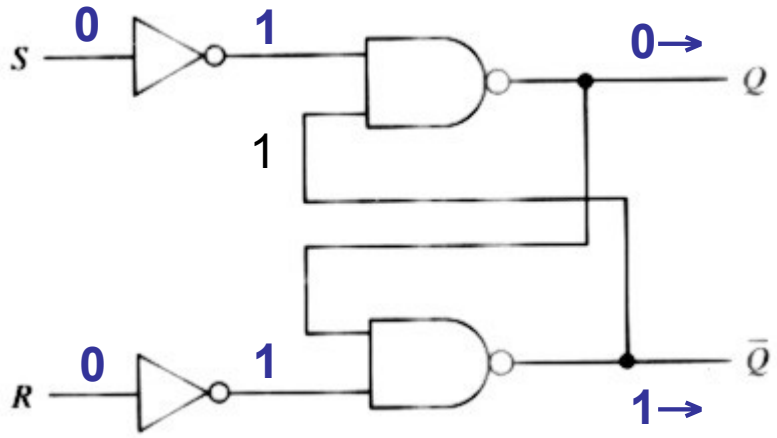
Análise de funcionamento do RS básico:

Condições de “repouso” (mantendo estado):

Condições iniciais:

S=0 Q(t)=0 ⟶ Próximo estado? Q(t+1)=?

R=0



(a)

A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

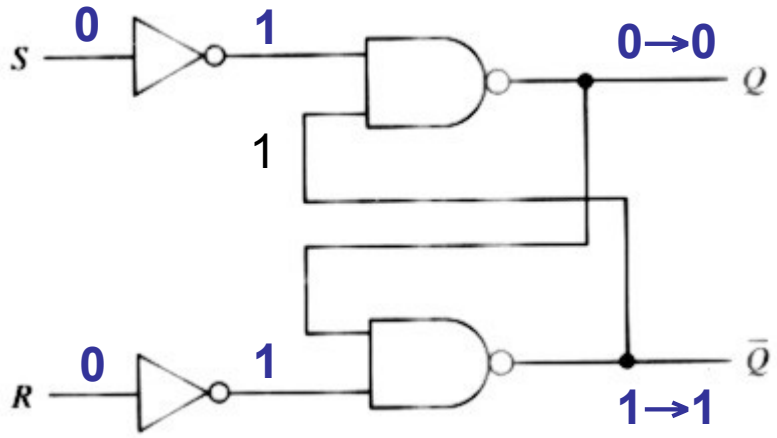
Análise de funcionamento do RS básico:

Condições de “repouso” (mantendo estado):

Condições iniciais:

S=0 Q(t)=0 ⟶ Próximo estado? Q(t+1)=?

R=0



(a)

A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

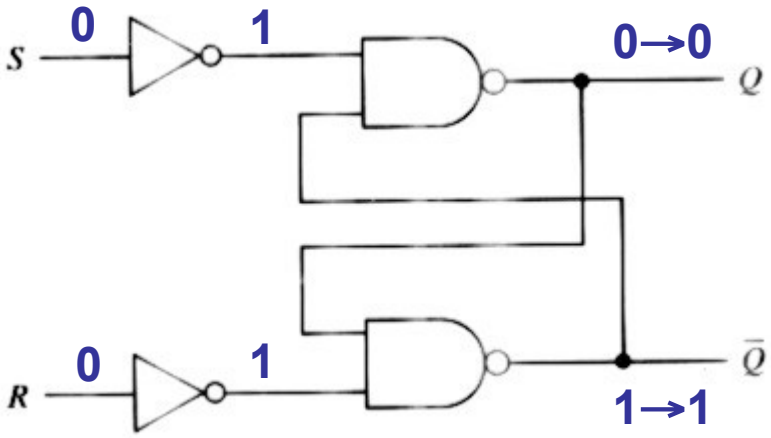
Análise de funcionamento do RS básico:

Condições de “repouso” (mantendo estado):

Condições iniciais:

S=0 Q(t)=0
R=0

→ Próximo estado? Q(t+1)=?

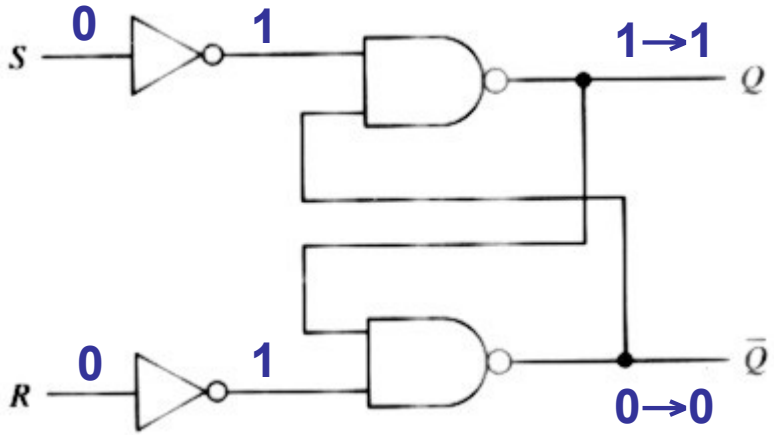


(a)

Condições iniciais:

S=0 Q(t)=1
R=0

→ Próximo estado? Q(t+1)=?



(b)

A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

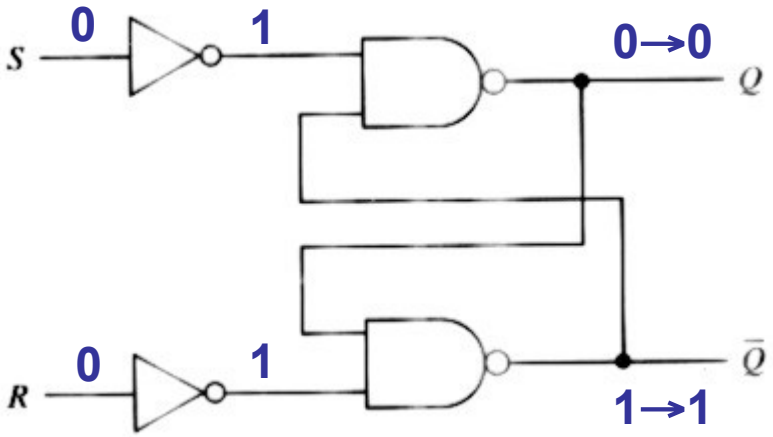
Análise de funcionamento do RS básico:

Condições de “repouso” (mantendo estado):

Condições iniciais:

S=0 Q(t)=0
R=0

→ Próximo estado? Q(t+1)=?

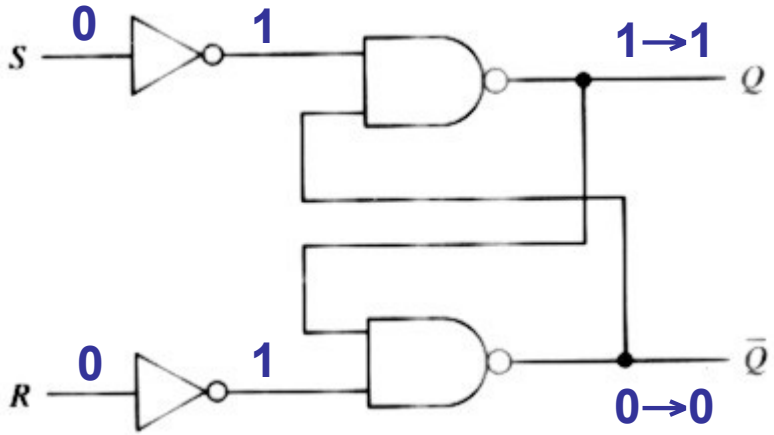


(a)

Condições iniciais:

S=0 Q(t)=1
R=0

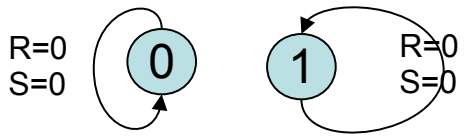
→ Próximo estado? Q(t+1)=?



(b)

Conclusões:

Set	Reset	Q(t+1)	Obs:
0	0	Q(t)	Mantêm estado. Não muda.



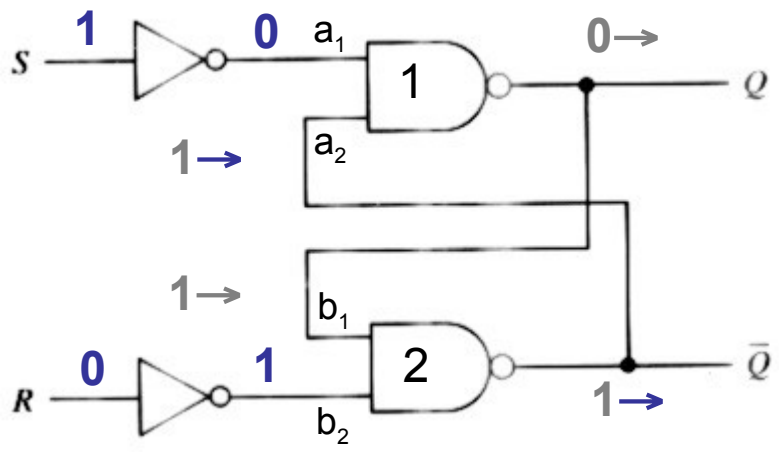
Análise de funcionamento do RS básico:

Setando o biestável:

Condições iniciais:

S=1
R=0
Q(t)=0

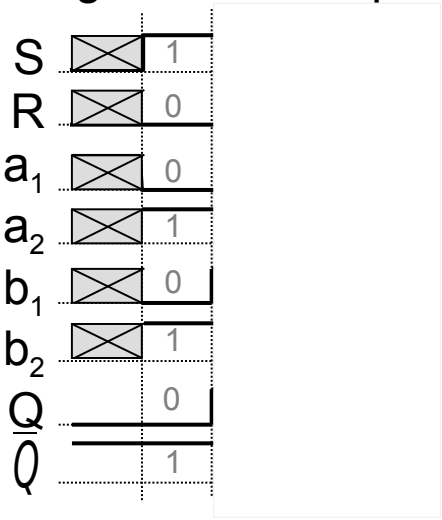
→ Próximo estado?
Q(t+1)=?



(a)

Obs: análise supondo que porta 1 é mais rápida que a porta 2.

Diagrama no tempo:



A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

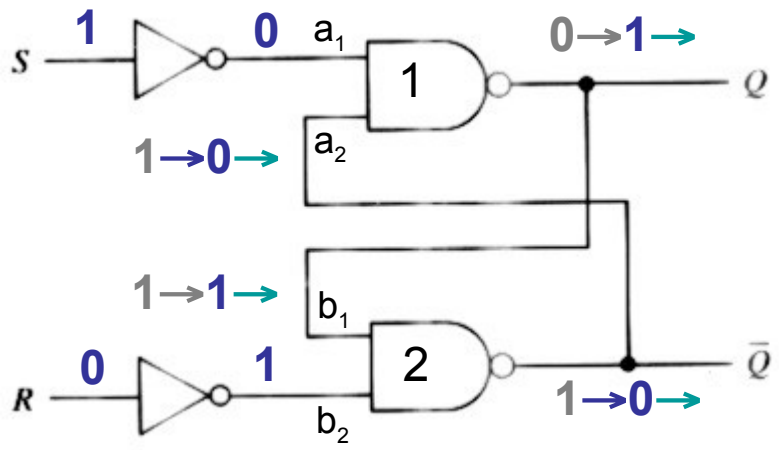
Análise de funcionamento do RS básico:

Setando o biestável:

Condições iniciais:

S=1 Q(t)=0 ⟶ Próximo estado? Q(t+1)=?

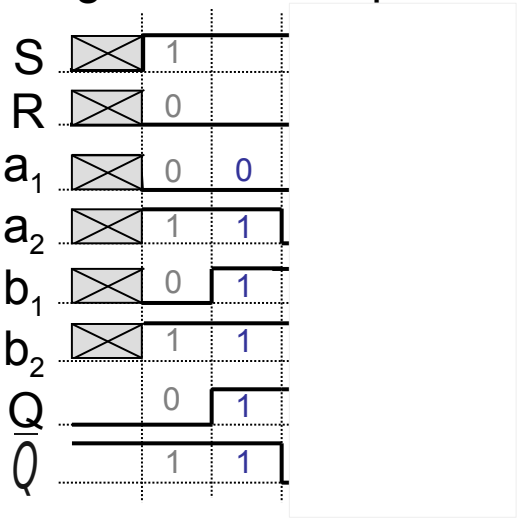
R=0



(a)

Obs: análise supondo que porta 1 é mais rápida que a porta 2.

Diagrama no tempo:



A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

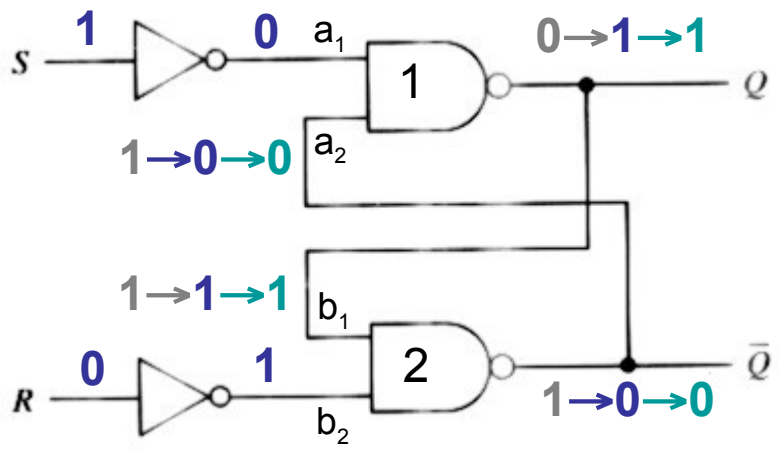
Análise de funcionamento do RS básico:

Setando o biestável:

Condições iniciais:

S=1 Q(t)=0 ⟶ Próximo estado? Q(t+1)=?

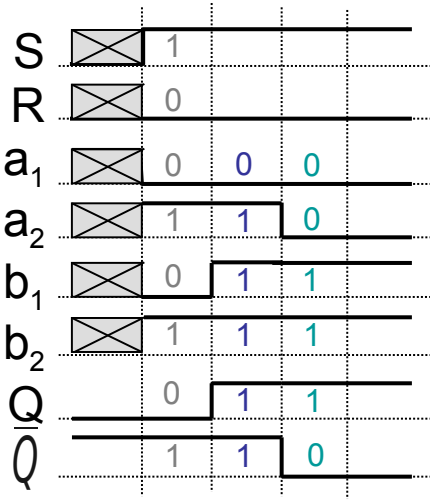
R=0



(a)

Obs: análise supondo que porta 1 é mais rápida que a porta 2.

Diagrama no tempo:



A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

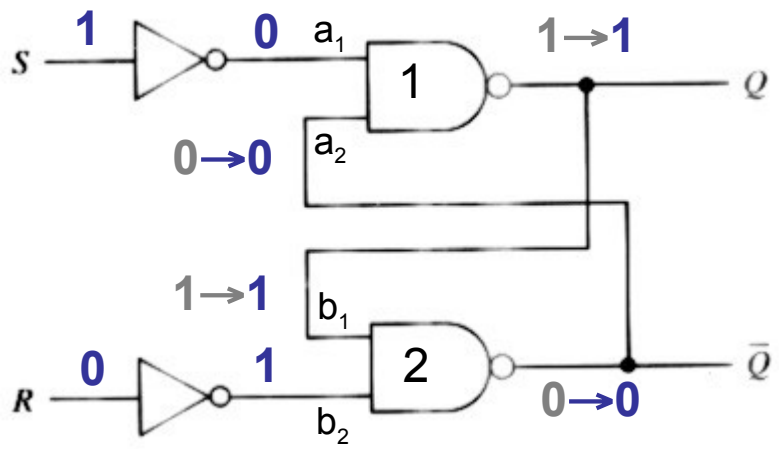
Análise de funcionamento do RS básico:

Setando o biestável:

Condições iniciais:

S=1
R=0
Q(t)=1

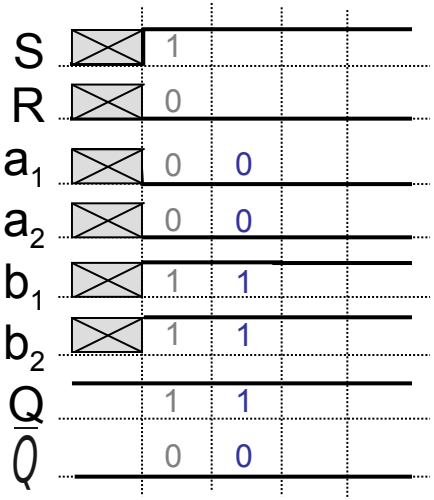
→ Próximo estado?
Q(t+1)=?



(b)

Obs: análise supondo que porta 1 é mais rápida que a porta 2.

Diagrama no tempo:



A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

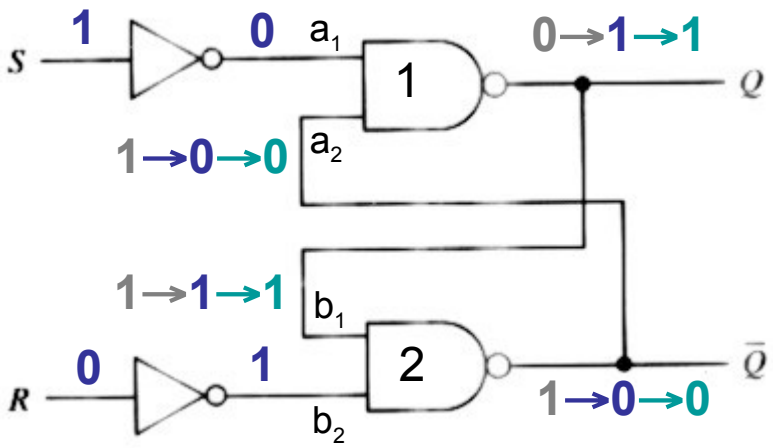
Análise de funcionamento do RS básico:

Setando o biestável:

Condições iniciais:

S=1 Q(t)=0 → Próximo estado? Q(t+1)=?

R=0

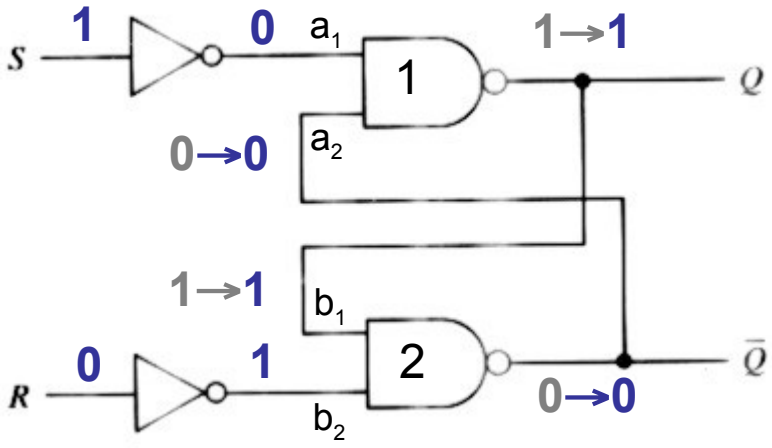


(a)

Condições iniciais:

S=1 Q(t)=1 → Próximo estado? Q(t+1)=?

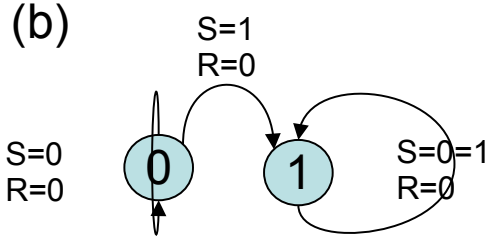
R=0



(b)

Conclusões:

Set	Reset	Q(t+1)	Obs:
0	0	Q(t)	Mantêm estado.
1	0	1	Set



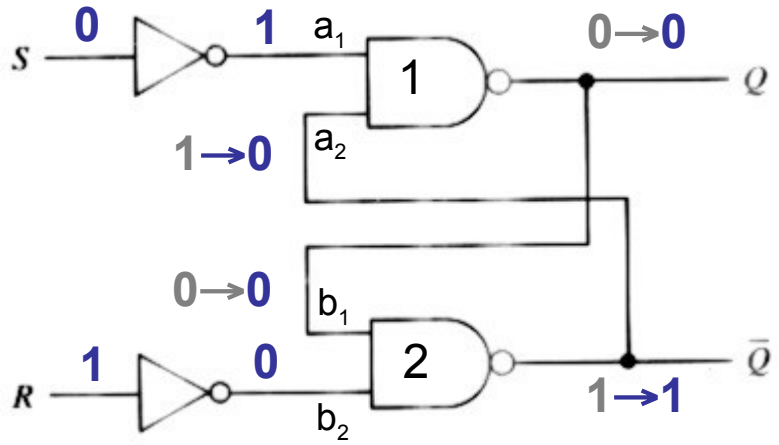
Análise de funcionamento do RS básico:

Resetando o biestável:

Condições iniciais:

S=0 Q(t)=0 ⟶ Próximo estado? Q(t+1)=?

R=1



(a)

Obs: análise supondo que porta 1 é mais rápida que a porta 2.

A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

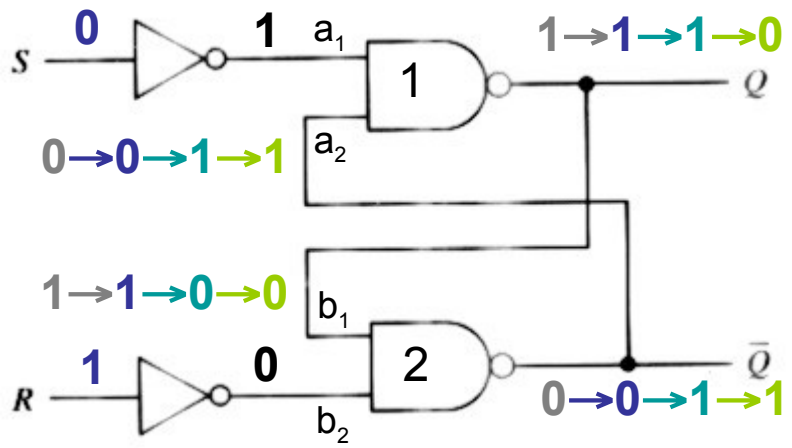
Análise de funcionamento do RS básico:

Resetando o biestável:

Condições iniciais:

S=0 Q(t)=1 ⟶ Próximo estado? Q(t+1)=?

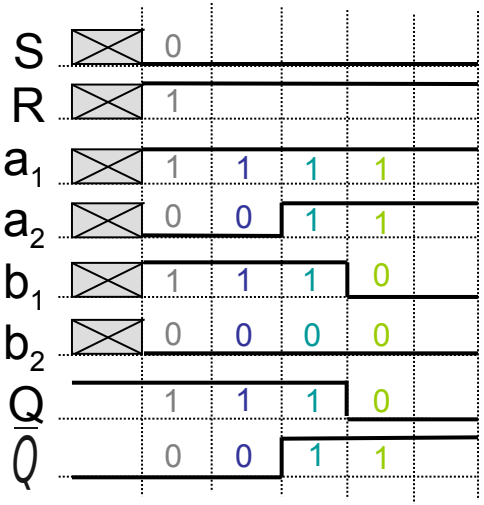
R=1



(b)

Obs: análise supondo que porta 1 é mais rápida que a porta 2.

Diagrama no tempo:



A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

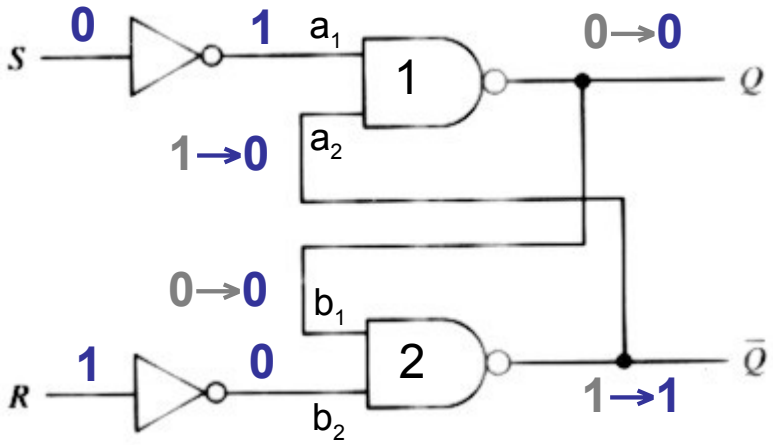
Análise de funcionamento do RS básico:

Resetando o biestável:

Condições iniciais:

S=0 Q(t)=0 → Próximo estado? Q(t+1)=?

R=1

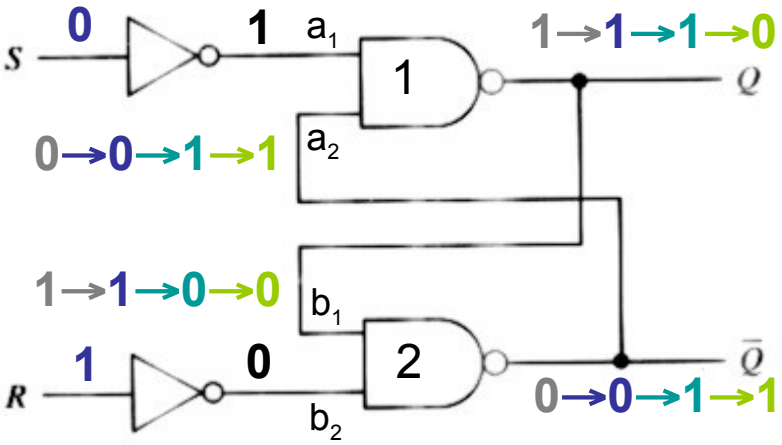


(a)

Condições iniciais:

S=0 Q(t)=1 → Próximo estado? Q(t+1)=?

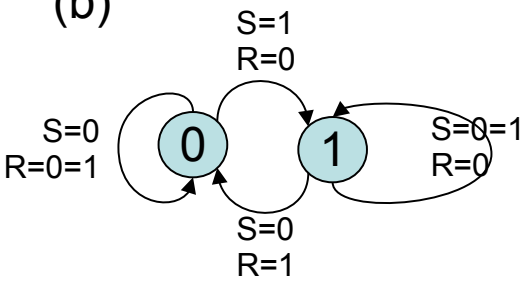
R=1



(b)

Conclusões:

Set	Reset	Q(t+1)	Obs:
0	0	Q(t)	Mantêm estado.
1	0	1	Set
0	1	0	Reset



Análise de funcionamento do RS básico:

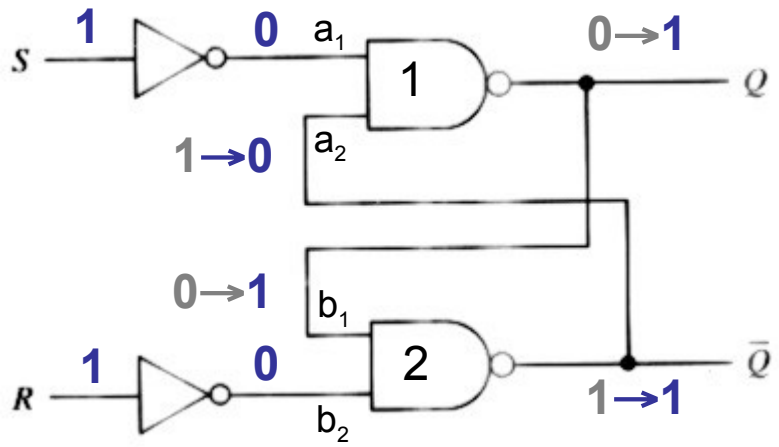
Setando e Resetando simultaneamente:

Condições iniciais:

S=1 Q(t)=0 → Q(t+1)=?

R=1

Próximo estado?

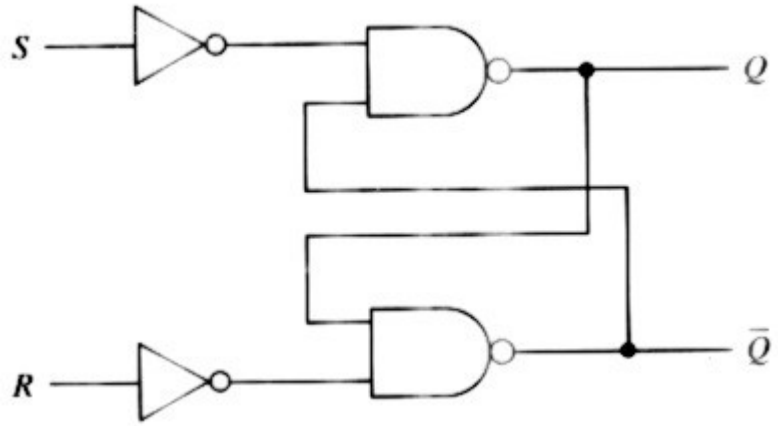


(a)

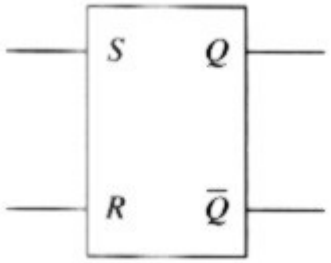
A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Biestável básico RS

Conclusões finais:



a) Circuito interno com portas NOT e NAND.

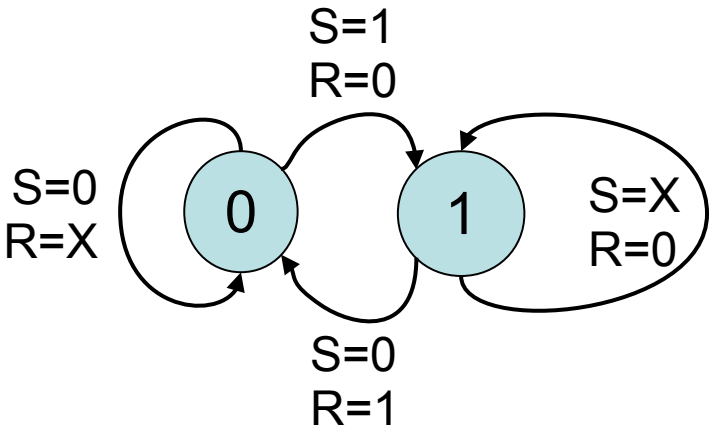


b) Símbolo do Biestável RS.

c) Tabela funcional:

Set	Reset	Q(t+1)	Obs:
0	0	Q(t)	Mantêm estado.
1	0	1	Set
0	1	0	Reset
1	1	1	Não utilizado* ($Q=\overline{Q}$)

d) Diagrama de estados:



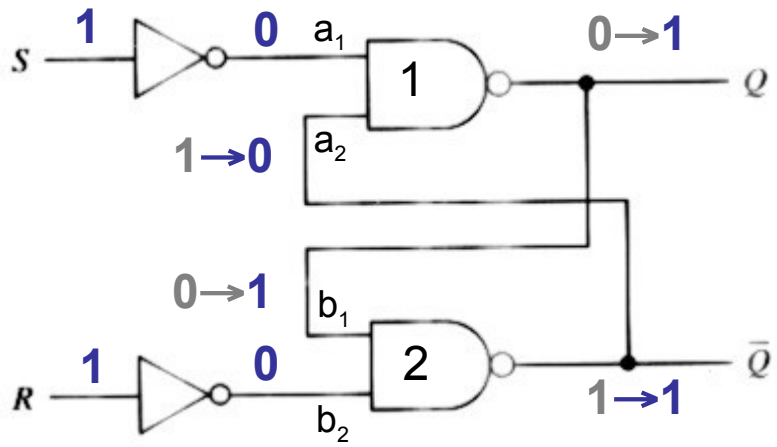
Análise de funcionamento do RS básico:

Setando e Resetando simultaneamente:

Condições iniciais:

S=1
R=1
Q(t)=0

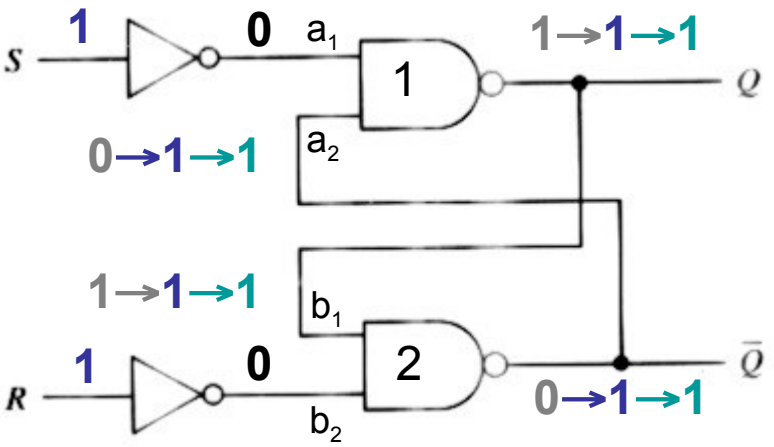
→ Próximo estado? Q(t+1)=?



Condições iniciais:

S=1
R=1
Q(t)=1

→ Próximo estado? Q(t+1)=?

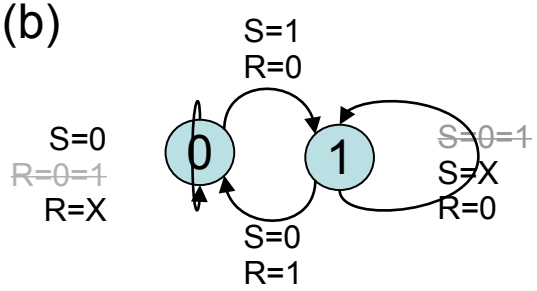


(a)

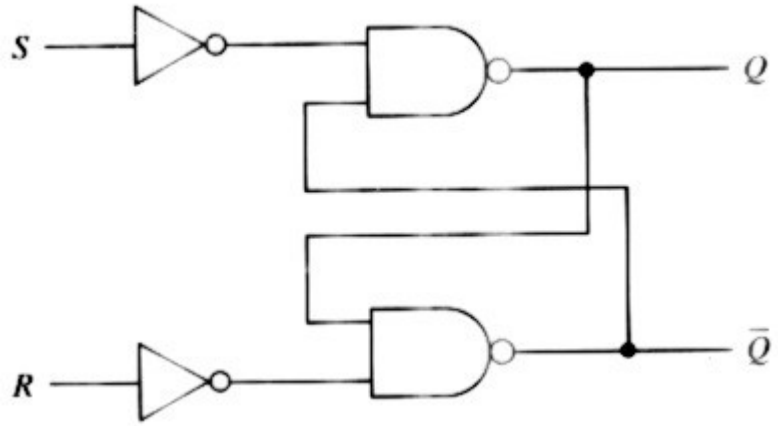
Conclusões:

Set	Reset	Q(t+1)	Obs:
0	0	Q(t)	Mantêm estado.
1	0	1	Set
0	1	0	Reset
1	1	1	Não utilizado* ($Q=\overline{Q}$)

(b)



Biestável básico RS

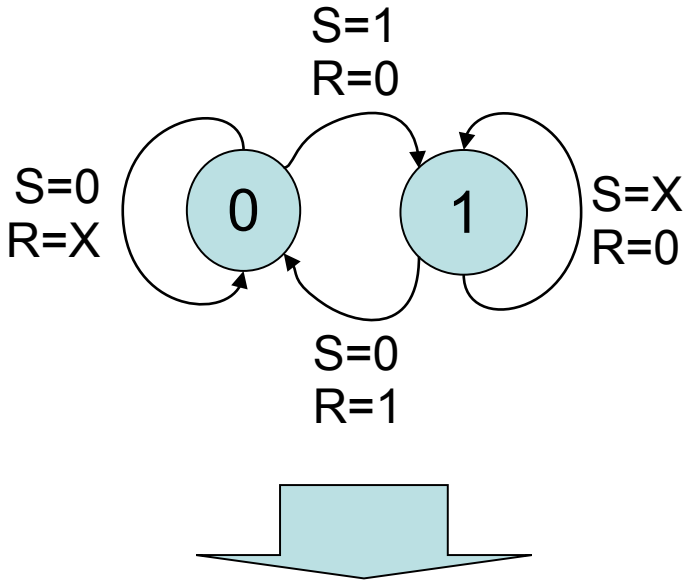


a) Circuito interno com portas NOT e NAND.

c) Tabela funcional:

Set	Reset	Q(t+1)	Obs:
0	0	Q(t)	Mantêm estado.
1	0	1	Set
0	1	0	Reset
1	1	1	Não utilizado* ($Q=\overline{Q}$)

d) Diagrama de estados:



e) Equação de transição:

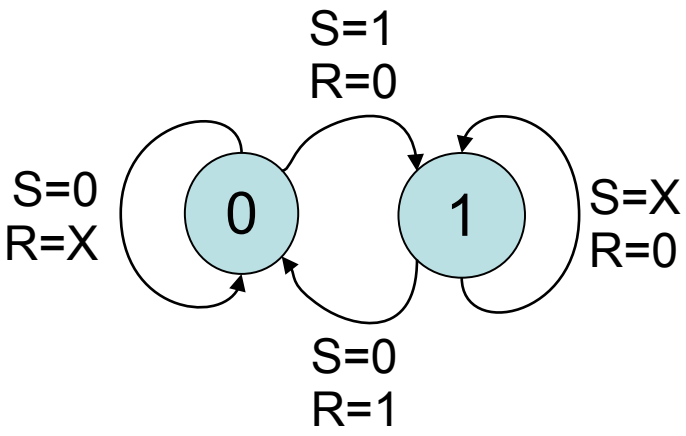
$$Q(t+1)=S(t)+\overline{R(t)}\cdot Q(t)$$

Biestável básico RS

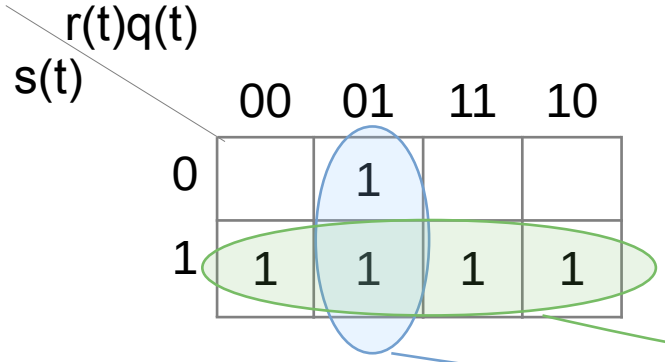
Dedução e. de transição:

Set	Reset	Q(t+1)	Obs:
0	0	Q(t)	Mantêm estado.
1	0	1	Set
0	1	0	Reset
1	1	1	Não utilizar: $Q(t+1)=\overline{Q}(t+1)$

d) Diagrama de estados:



Q(t+1):

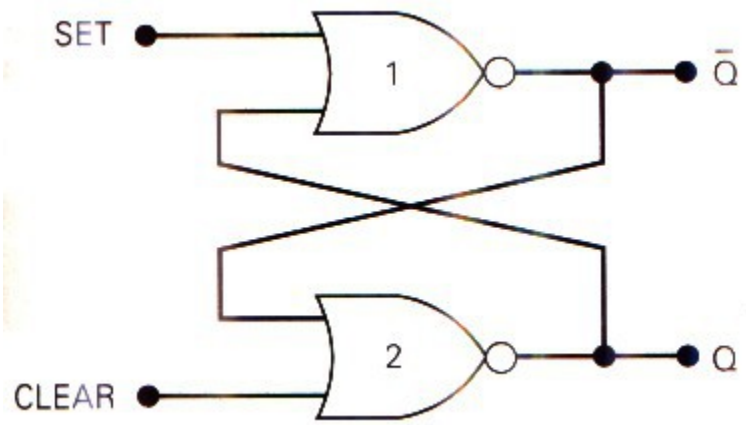


e) Equação de transição:

$$Q(t+1)=S(t)+\overline{R(t)}\cdot Q(t)$$

Outros biestáveis RS:

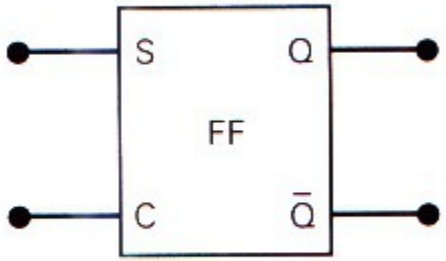
Biestável RS básico com portas NOR:



Set	Clear	Saída
0	0	Não muda
1	0	Q = 1
0	1	Q = 0
1	1	Inválida*

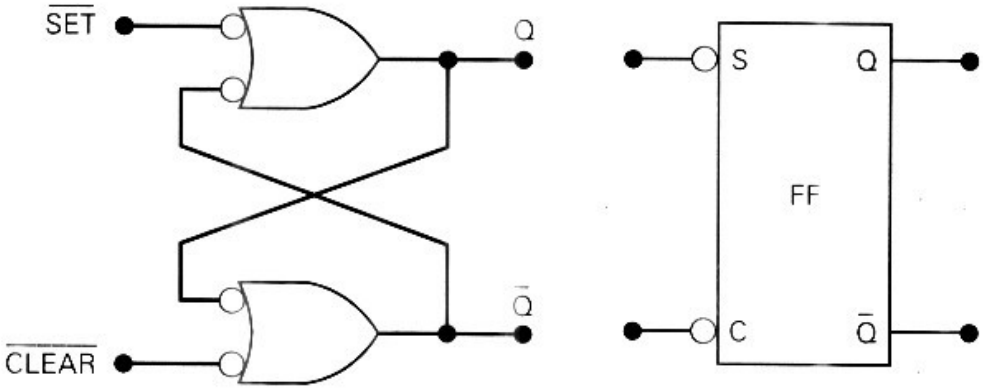
*produz $Q = \bar{Q} = 0$

(b)



(c)

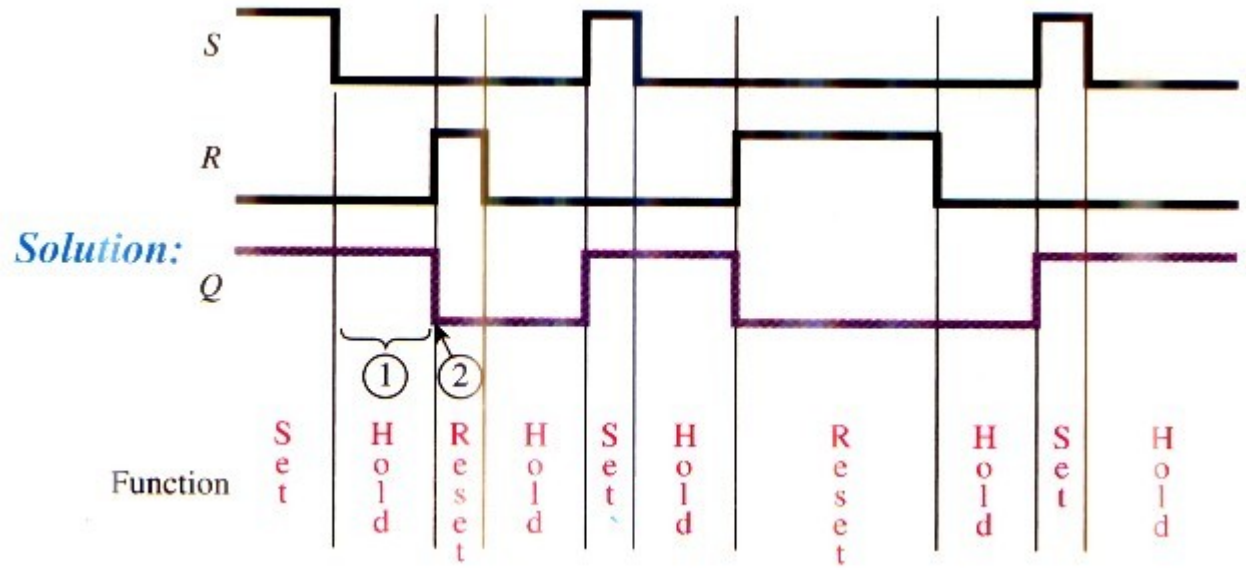
Biestável RS com portas NOT+OR:

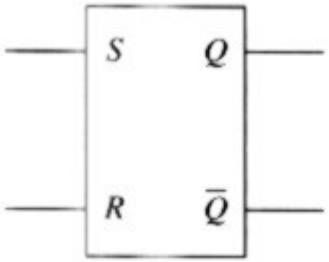


Biestável RS:

Exemplo de uso:

Set	Reset	Q(t+1)	Obs:
0	0	Q(t)	Mantêm estado.
1	0	1	Set
0	1	0	Reset
1	1	1	Condição inválida

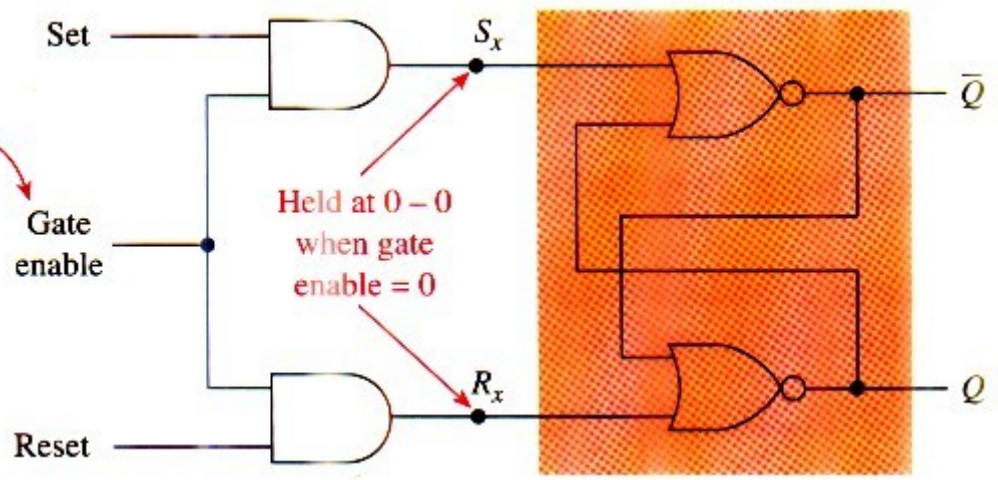




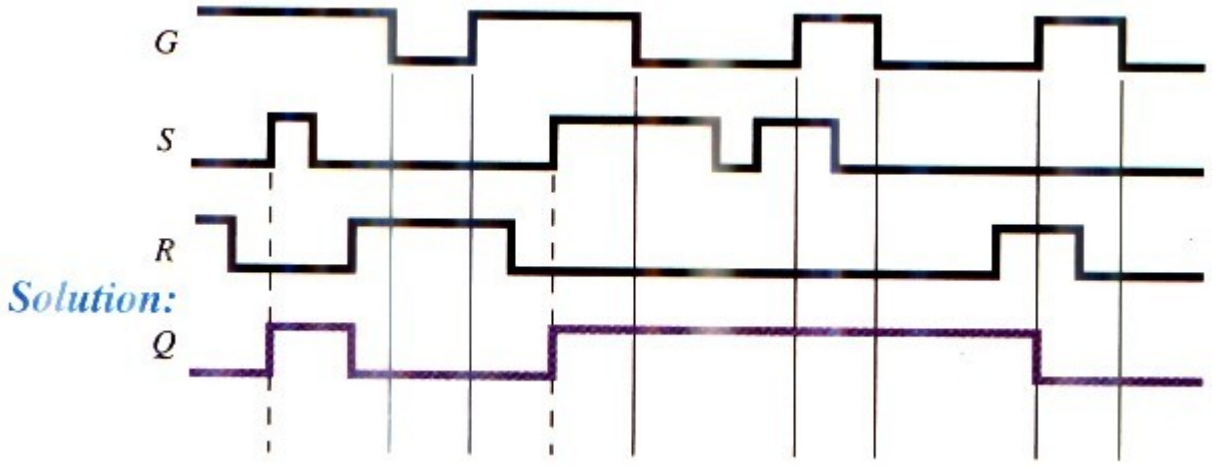
Latch RS

Biestável com entrada de ENABLE:

Nível lógico ALTO permite que níveis lógicos introduzidos nos pinos "Set" e "Reset" passem para dentro do biestável.

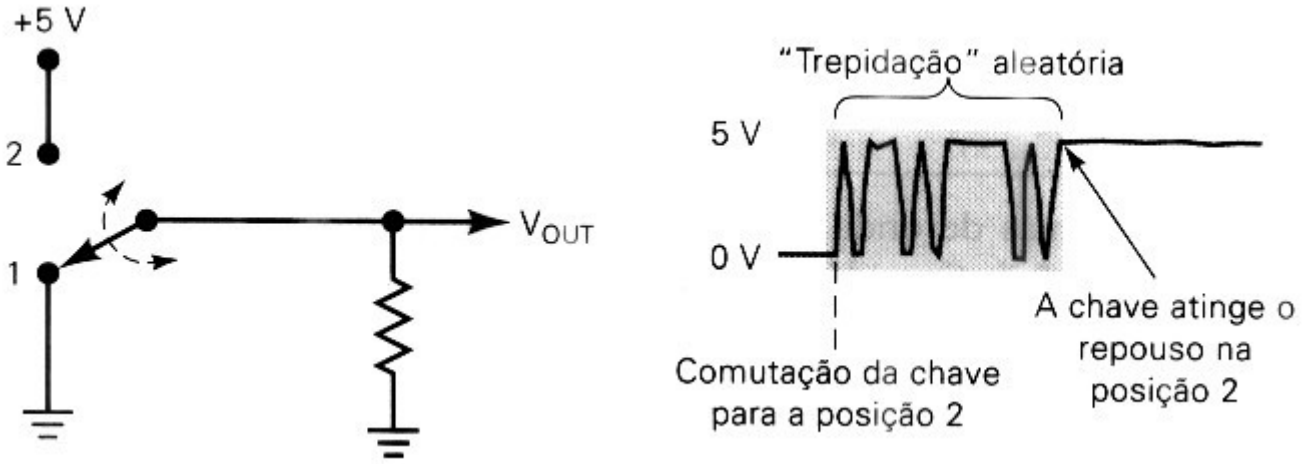


Biestável RS.



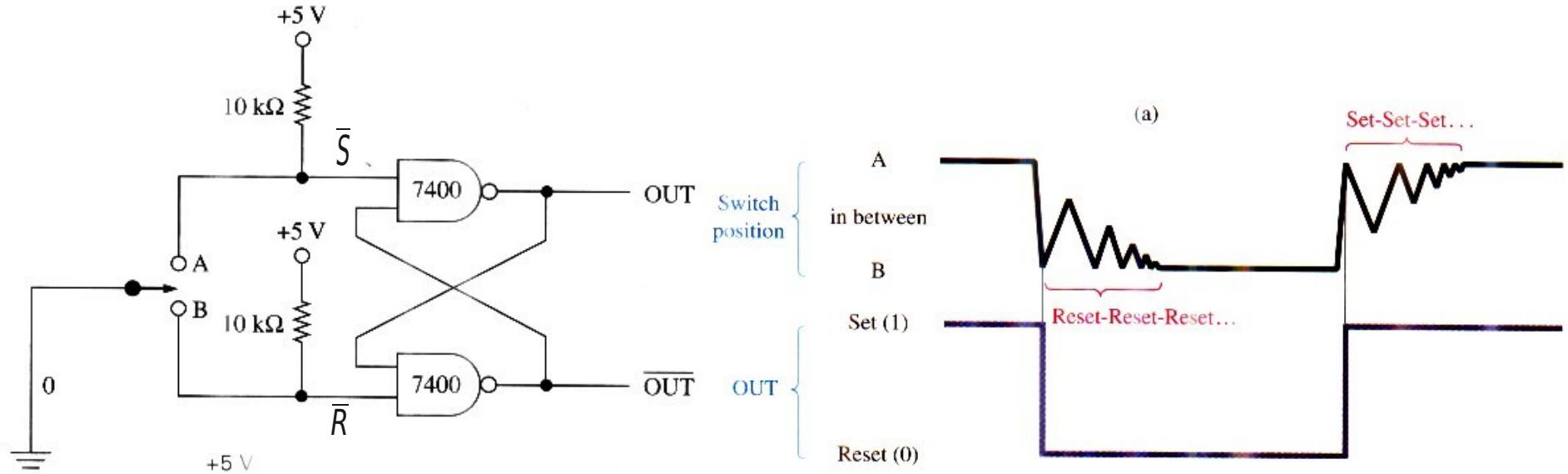
Aplicação de biestável RS

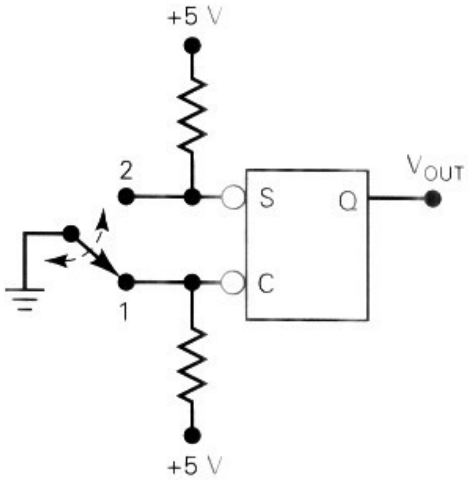
Circuito problema do efeito "*bouncing*" de chaves:



Aplicação de biestável RS

Circuito para eliminar efeito "*bouncing*" de chaves:

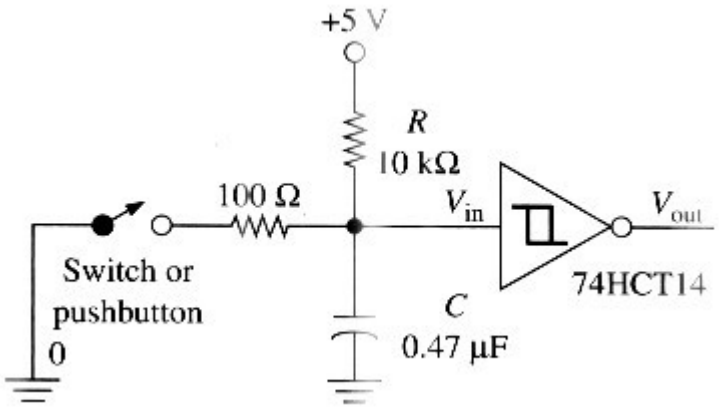




$\overline{S}$	$\overline{R}$	Set	Reset	Q(t+1)	Obs:
1	1	0	0	Q(t)	Mantêm estado.
0	1	1	0	1	Set
1	0	0	1	0	Reset
0	0	1	1	1	Condição inválida – não ocorre.

Circuitos de Debouncing

Outro circuito empregando Schmitt-trigger:



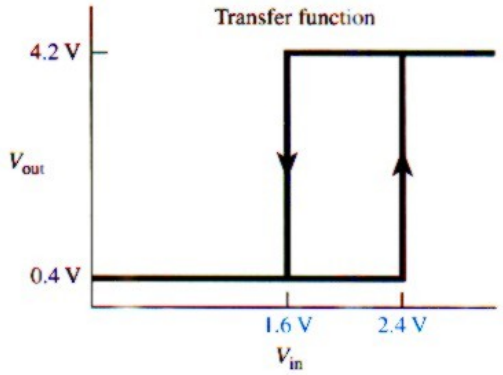
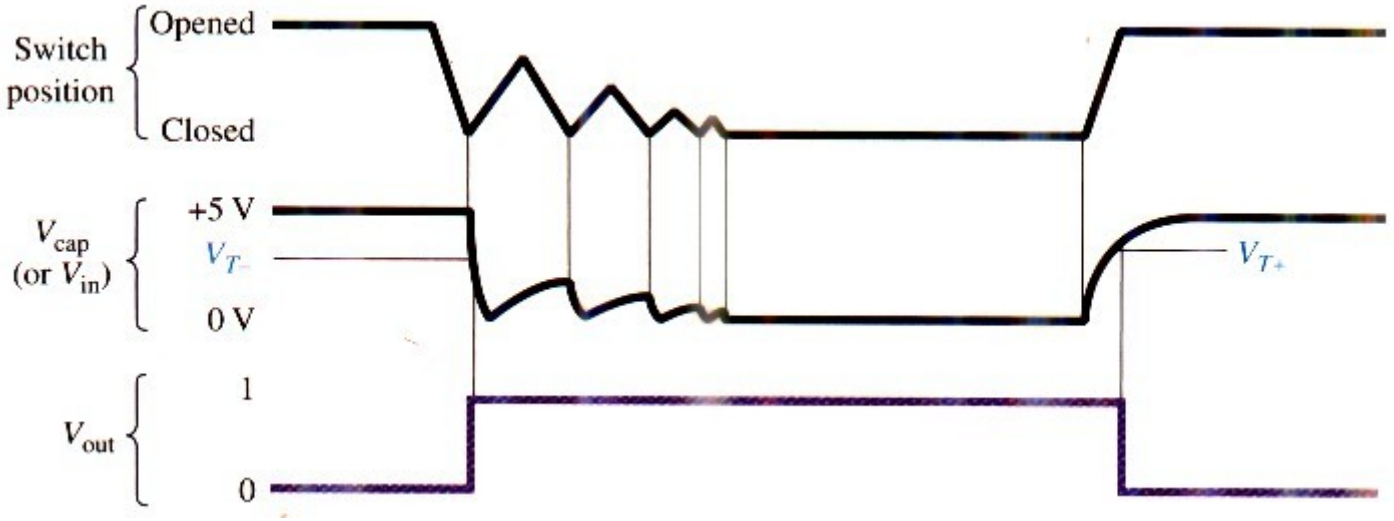
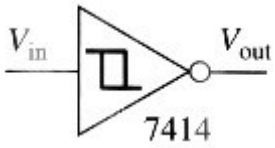


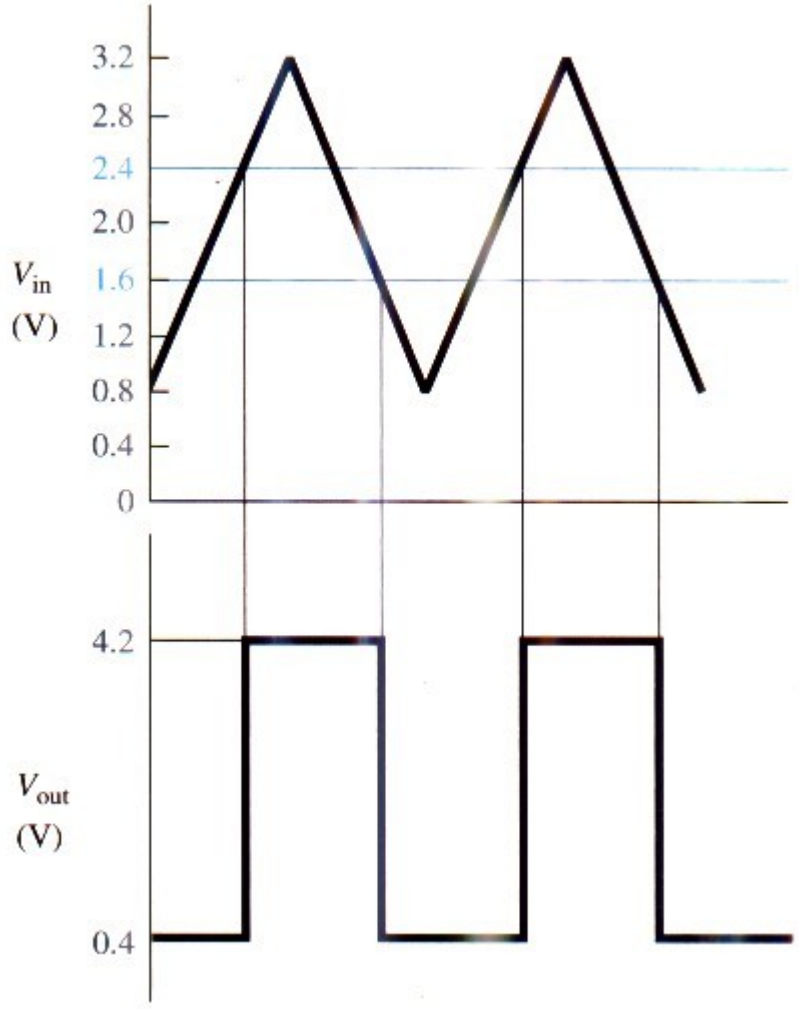
Fig.: Função transferência do Schmitt-trigger.



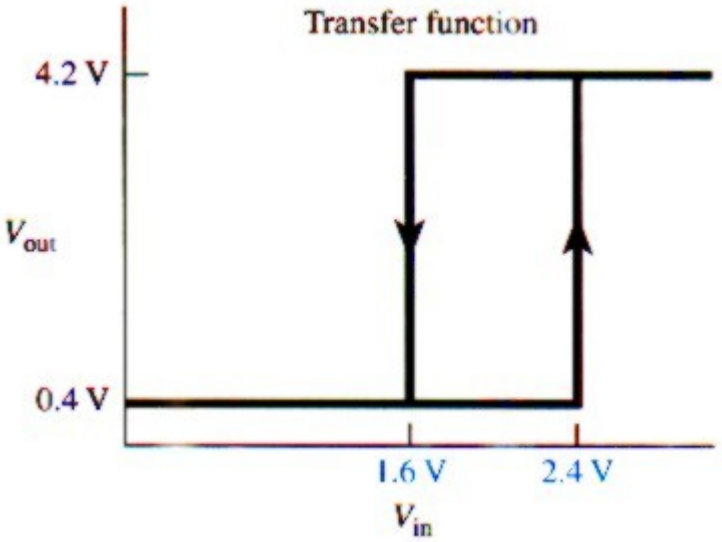
Operação de um Schmitt trigger:

Ex.: 7414:

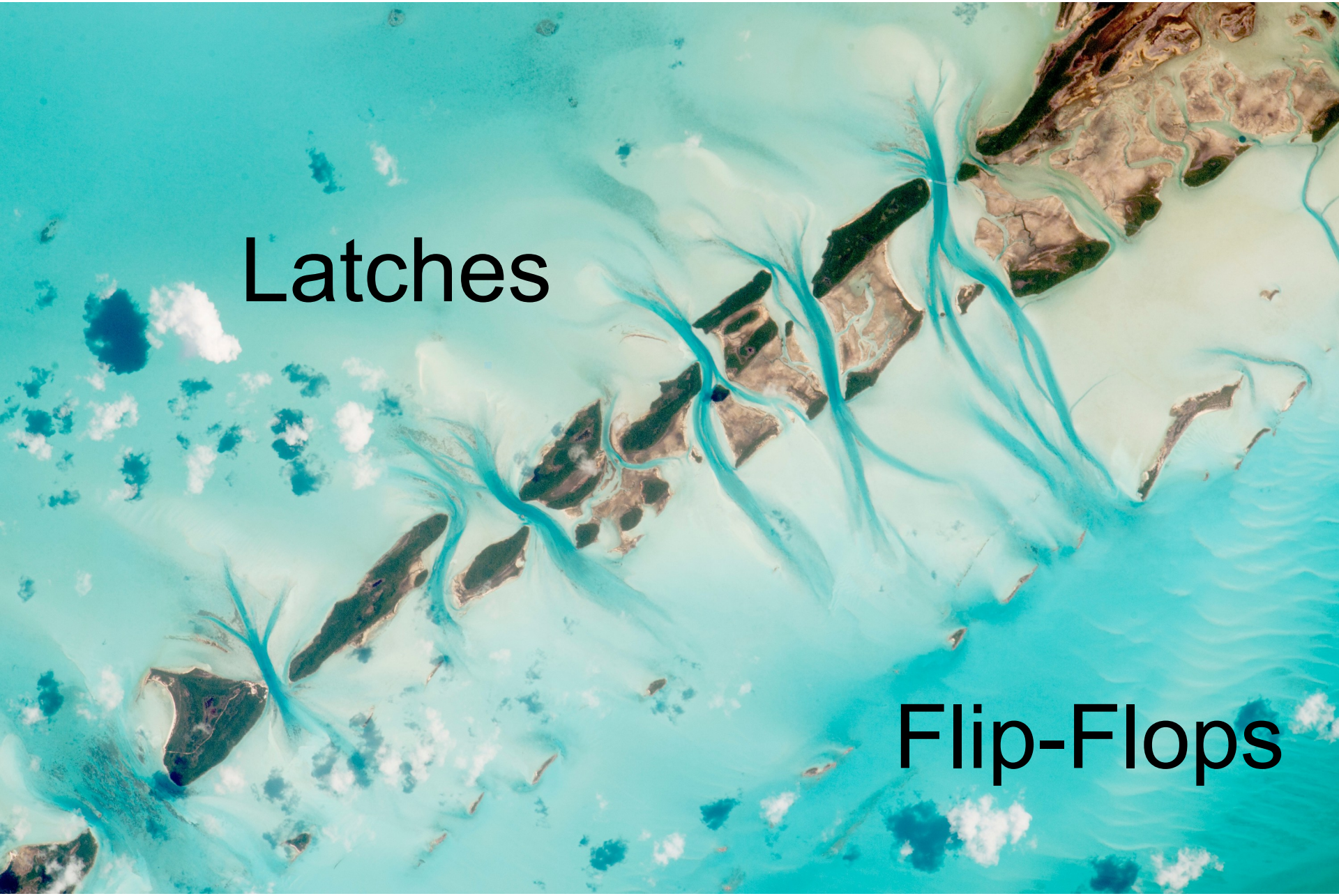




a) Simulação de Schmitt-trigger.

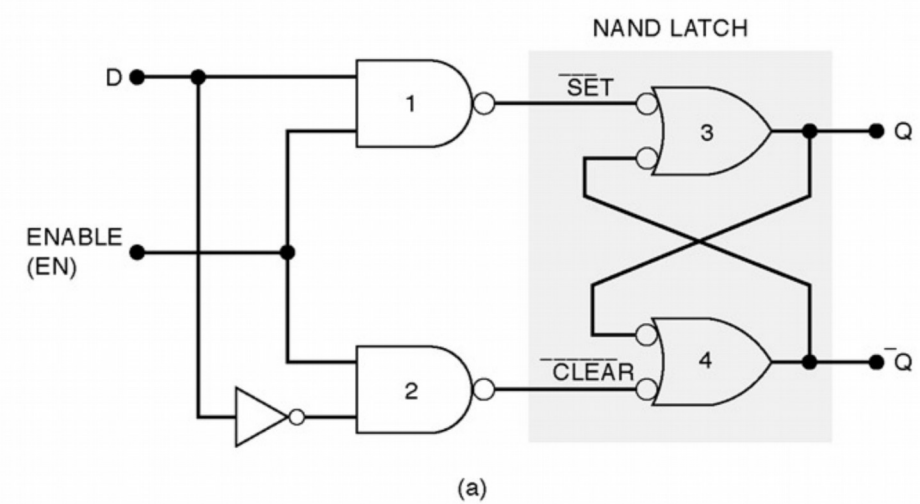


b) Função transferência.


Latches
Flip-Flops

Latches x Flip_Flops: Biestáveis

- **Latch**: entrada "extra" (Enable) sensível à nível lógico:

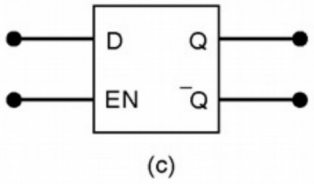


Inputs		Output	
EN	D	Q	
0	X	Q_0 (no change)	← "hold
1	0	0	
1	1	1	

"X" indicates "don't care"
Q_0 is state Q just prior to EN going LOW

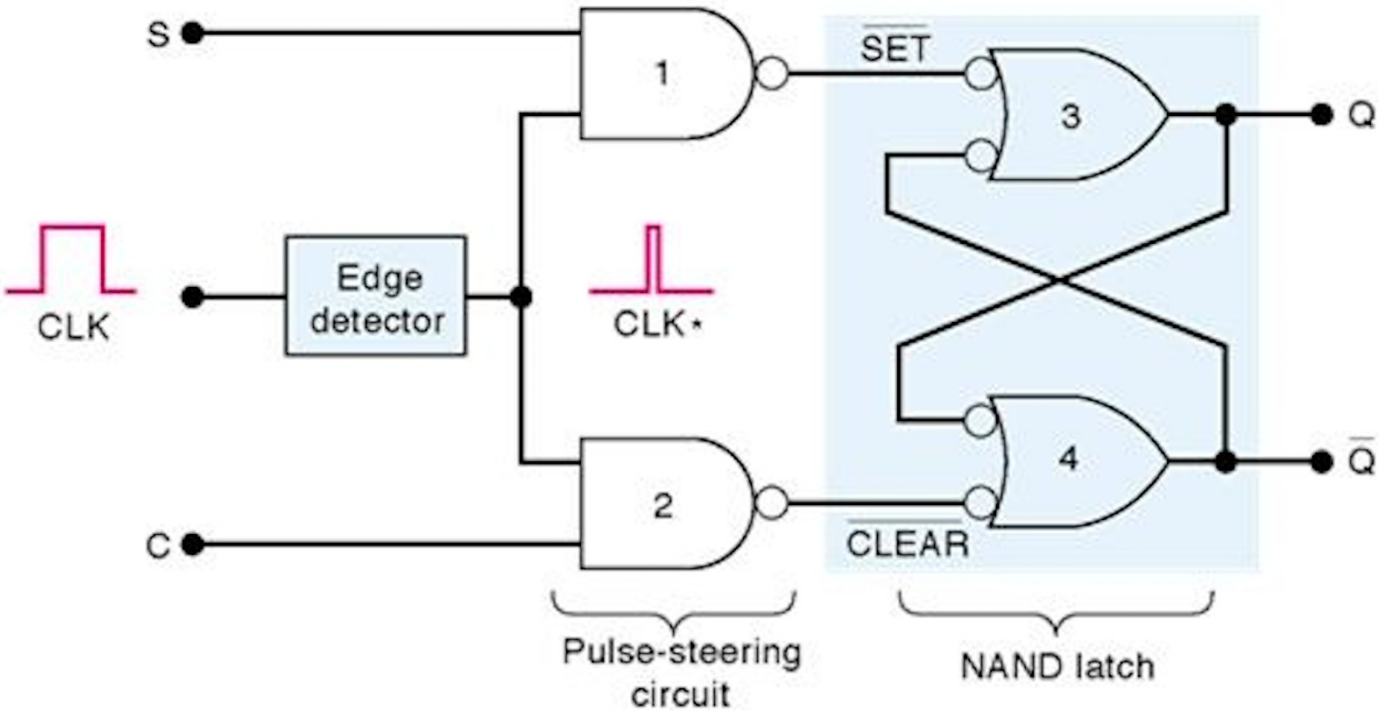
(b)

Fig.: D Latch (transparent latch)



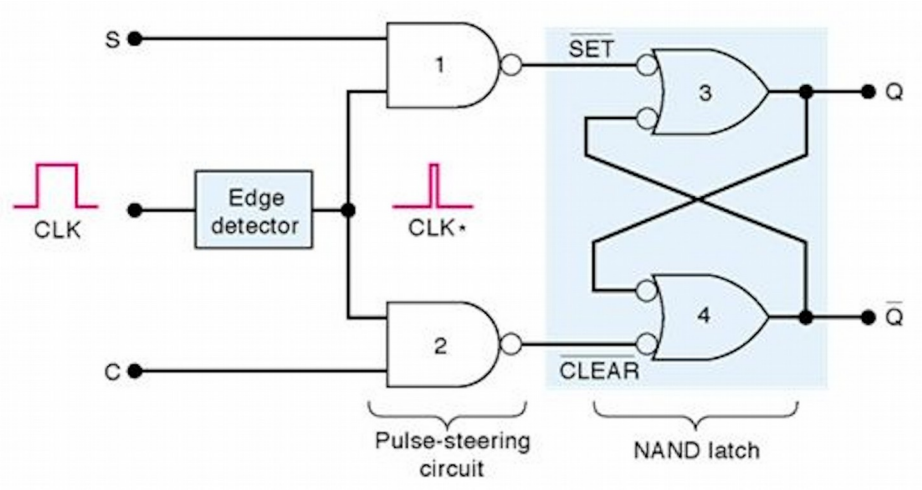
Latches x Flip_Flops: Biestáveis

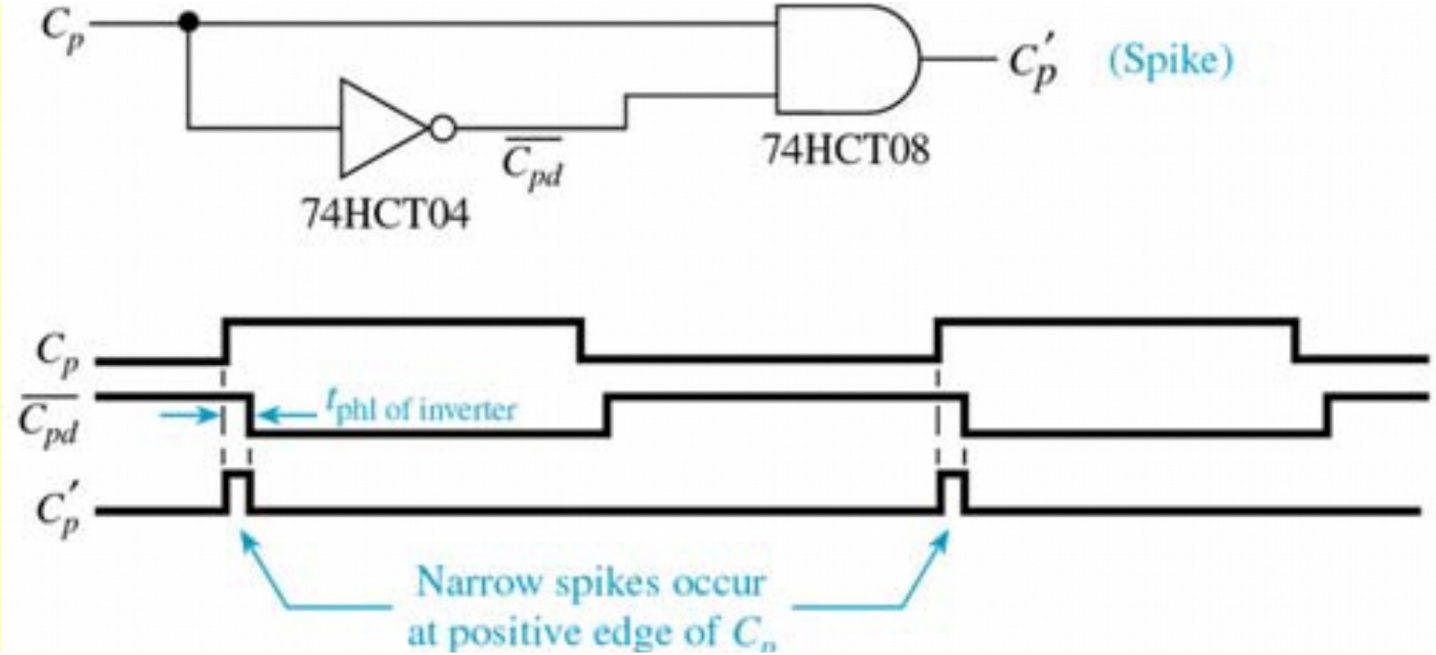
- **Flip-Flop**: entrada “extra” (Clock) sensível à borda do sinal (nesta entrada):



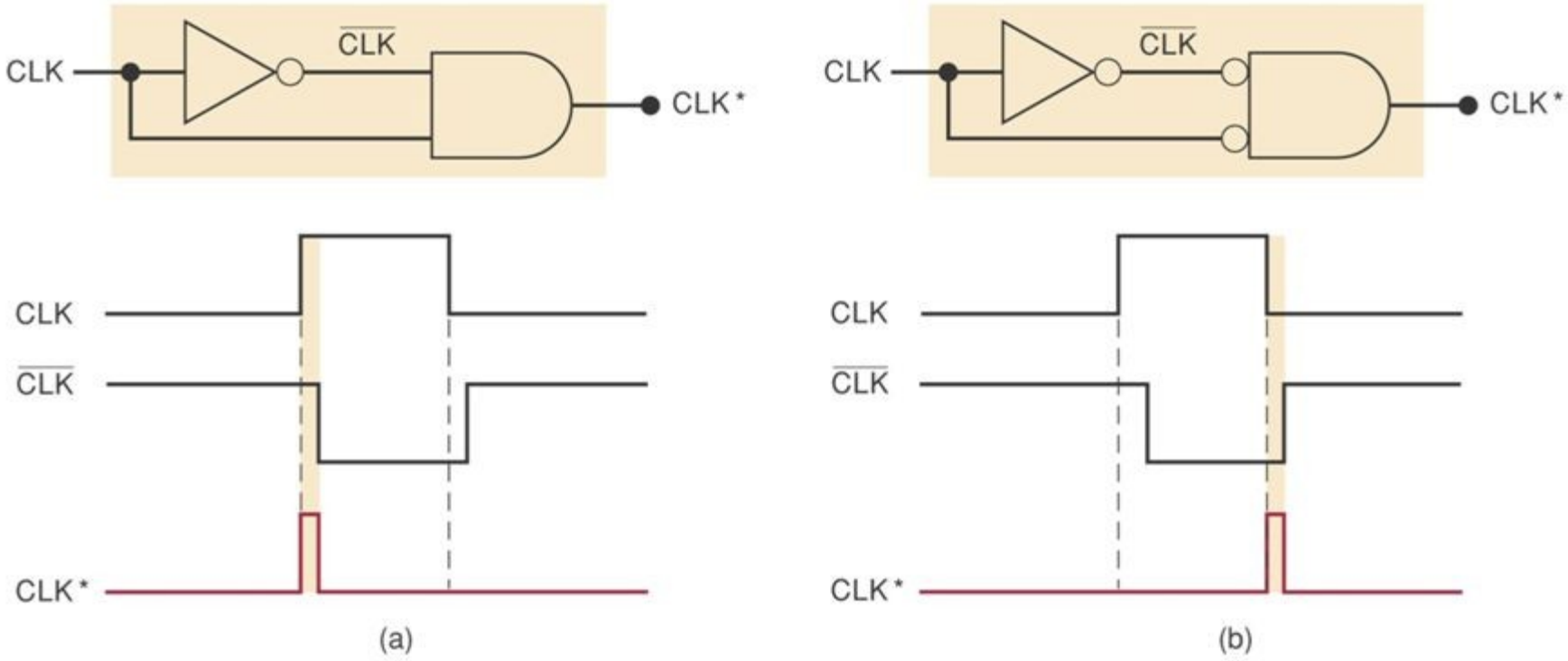
Detector de bordas

- “Positive edge-detection circuit”

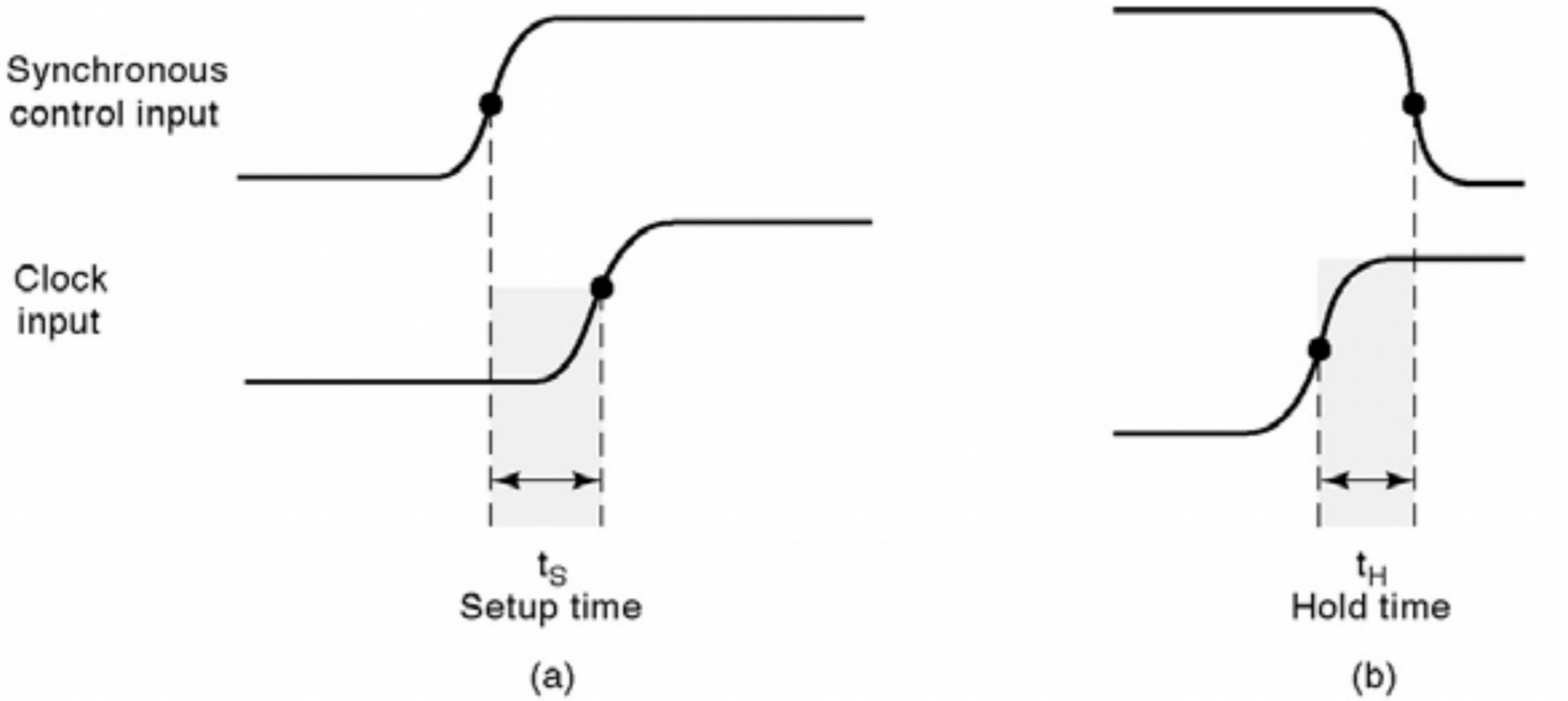




Detectores de Bordas



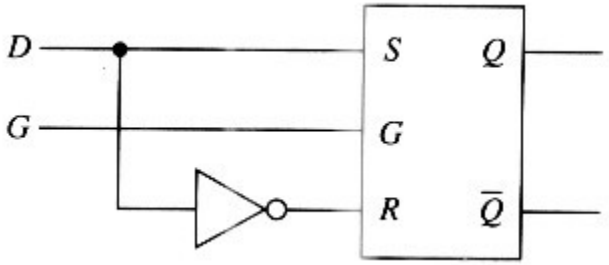
Parâmetros no tempo:



Latch Tipo D:

Tabela verdade do RS:

Set	Reset	Q(t+1)	Obs:
0	0	Q(t)	Mantêm estado.
1	0	1	Set
0	1	0	Reset
1	1	1	Condição inválida

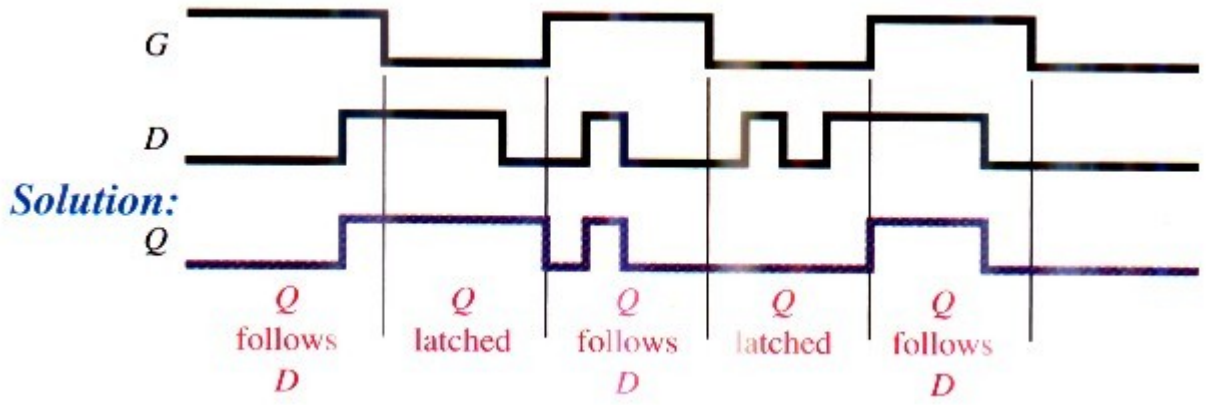


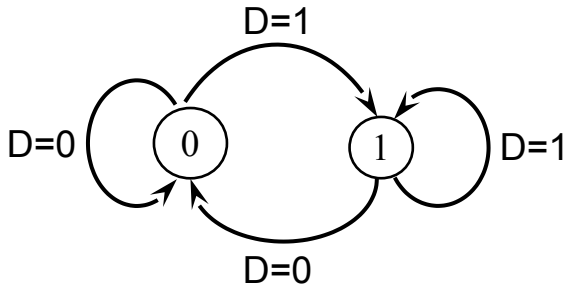
(a) Circuito interno.

b) Tabela verdade do Latch D:

G	D	Q(t+1)	Obs:
0	X	Q(t)	Mantêm estado.
1	**0**	**1**	Reset
1	**1**	**1**	Set

d) Simulação no tempo:

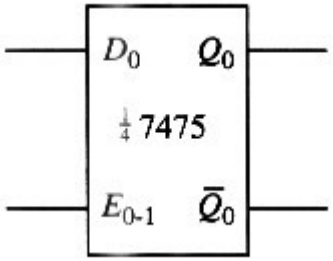


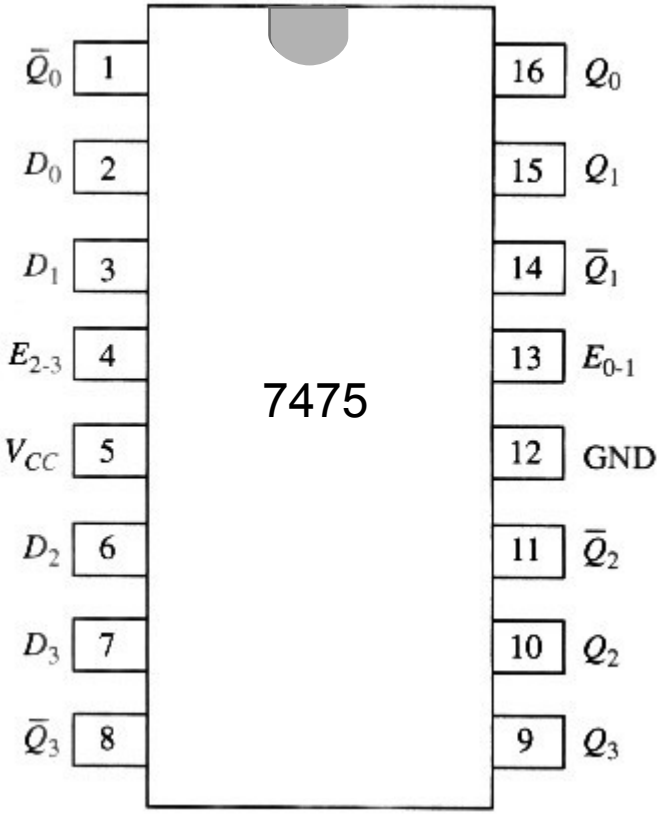


c) Diagrama de estados.

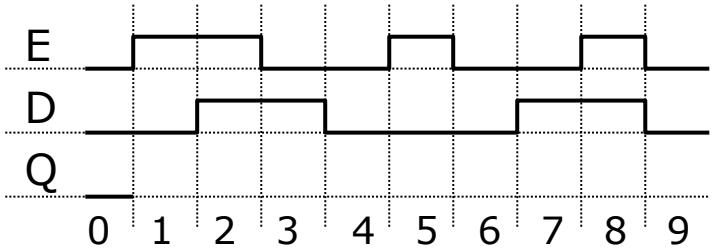
Latch D

CI comercial:





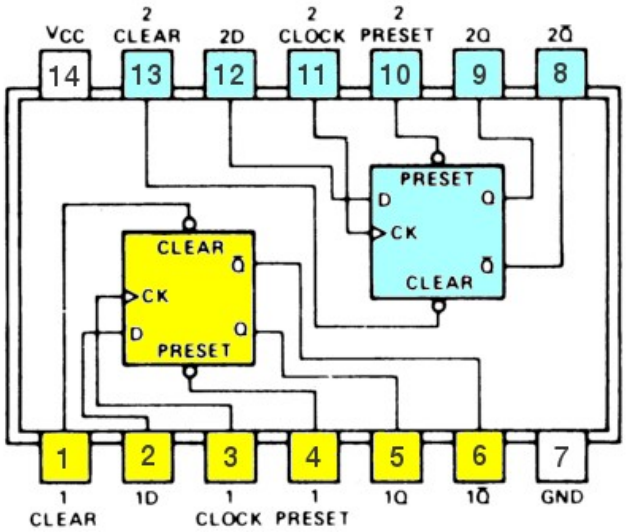
Completar:

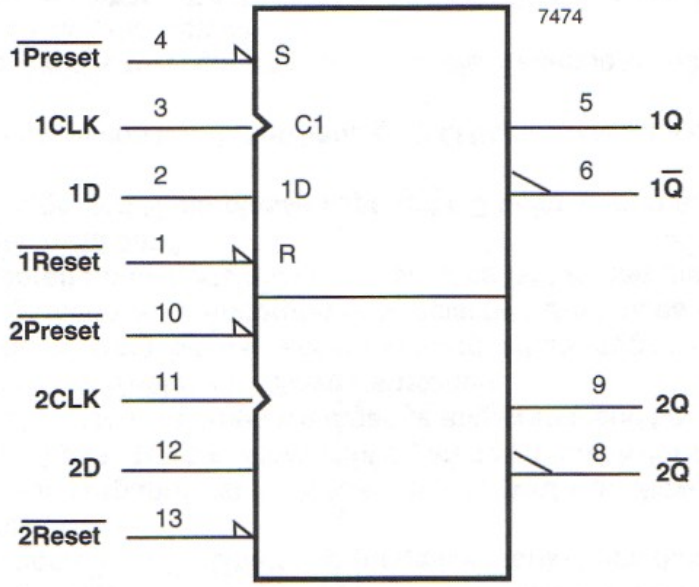


Biestáveis D comerciais

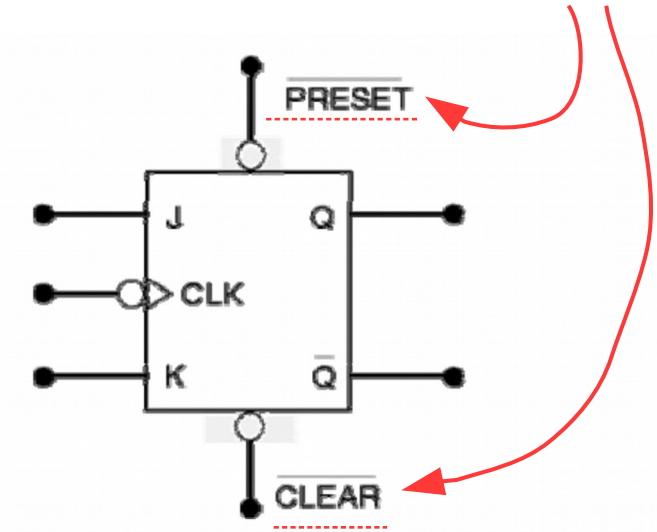
- 7474: Flip-Flop D,
- 7475: Latch D,

74LS74
Flip-Flop





Entradas assíncronas...

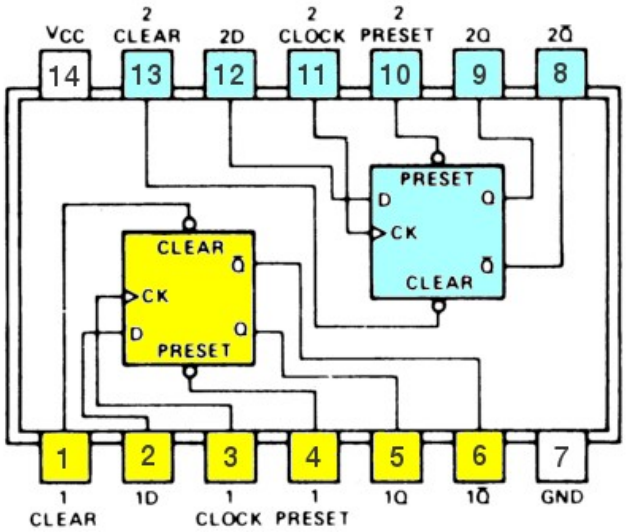


PRESET	CLEAR	FF response
1	1	Clocked operation*
0	1	Q = 1 (regardless of CLK)
1	0	Q = 0 (regardless of CLK)
0	0	Not used

*Q will respond to J, K, and CLK

- Num FF-D ou FF-JK, as entradas D, J ou K são ditas "síncronas" porque seu efeito na saída do FF depende da sincronização com o sinal de "clock".
- Entradas assíncronas ($\overline{PRESET}$, $\overline{CLEAR}$): sobre-escrevem as entradas síncronas; operam de forma independente das entradas síncronas e do sinal de clock e são usadas para ajustar ("forçar") um FF para o estado 0 ou 1 em qualquer instante de tempo (principalmente quando recém se alimenta um circuito, para garantir sua condição inicial).

74LS74
Flip-Flop



AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

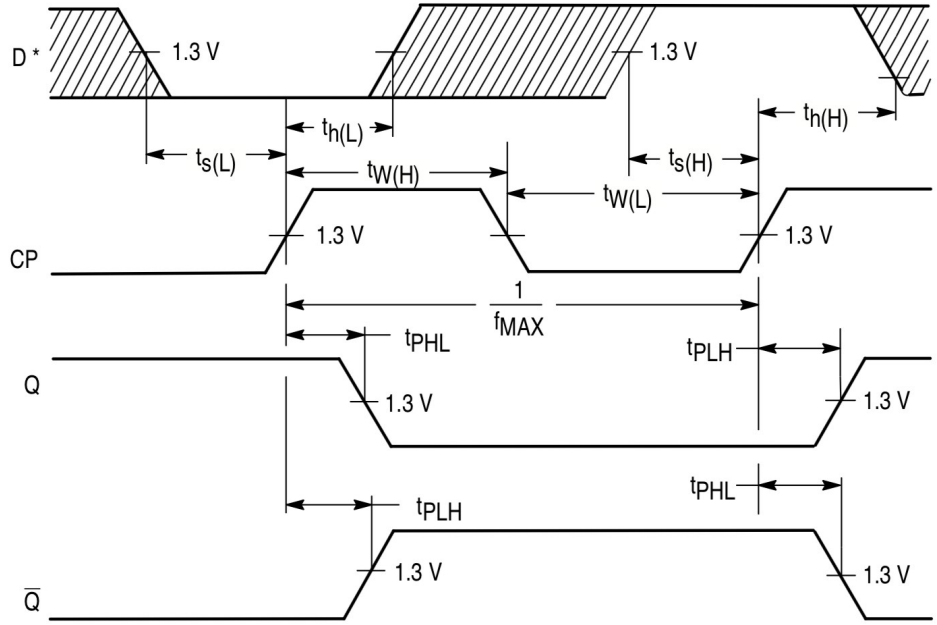
Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
f_{MAX}	Maximum Clock Frequency	25	33		MHz	Figure 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Clock, Clear, Set to Output		13	25	ns	Figure 1	
			25	40	ns		

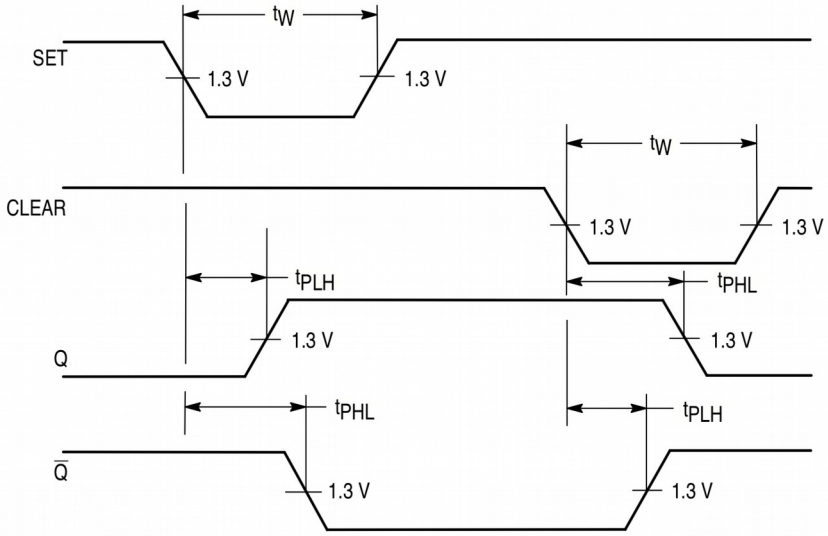
AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
$t_{W(H)}$	Clock	25			ns	Figure 1	V_{CC} = 5.0 V
$t_{W(L)}$	Clear, Set	25			ns	Figure 2	
t_s	Data Setup Time — HIGH	20			ns	Figure 1	
	LOW	20			ns		
t_h	Hold Time	5.0			ns	Figure 1	

Parâmetros AC

AC WAVEFORMS





*The shaded areas indicate when the input is permitted to change for predictable output performance.

t_{PLH} t_{PHL}	Clock, Clear, Set to Output		13 25	25 40	ns ns	Figure 1	V_{CC} = 5.0 V C_L = 15 pF

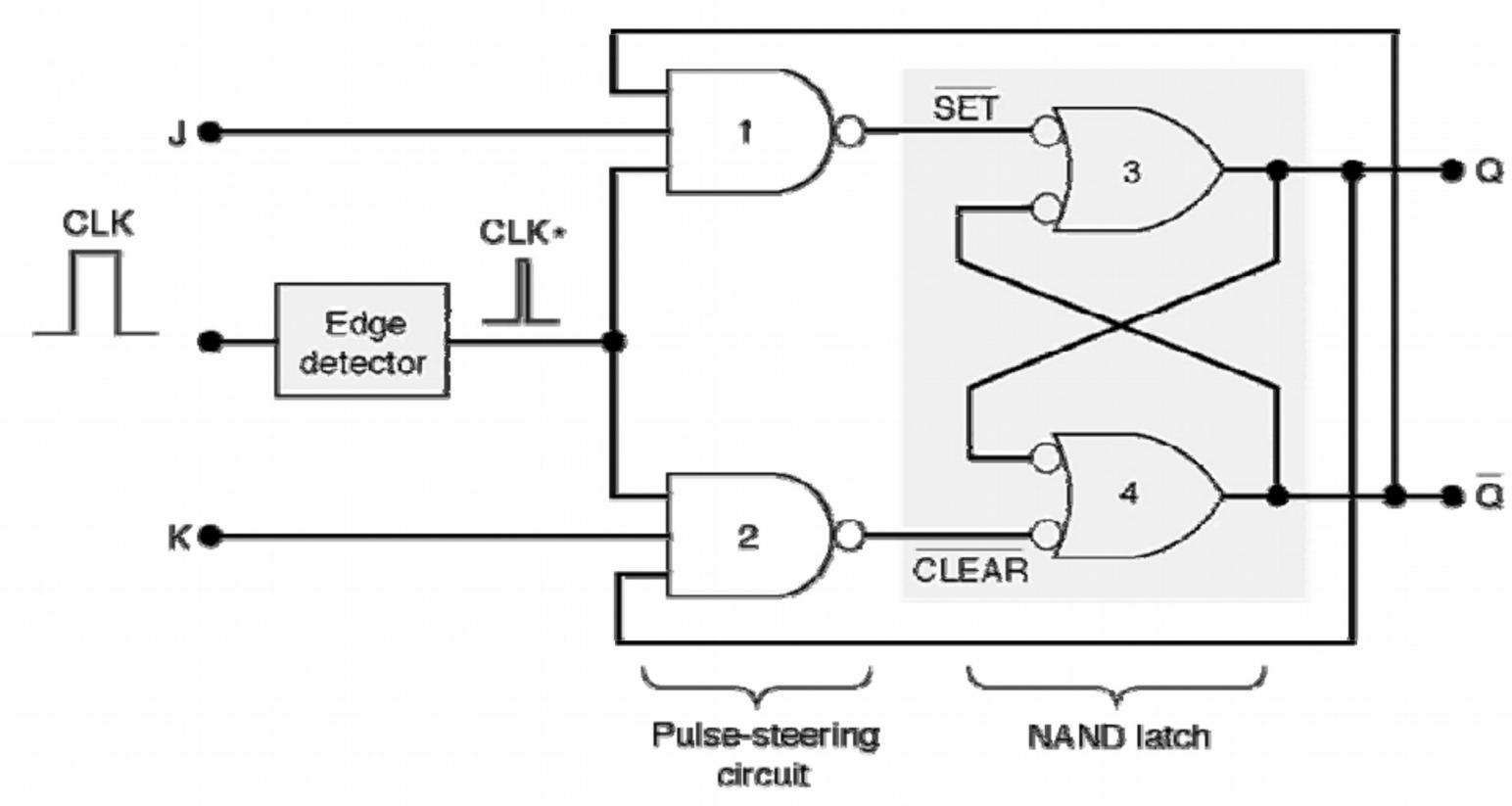
AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions	
$t_{W(H)}$	Clock	25			ns	Figure 1	V_{CC} = 5.0 V
$t_{W(L)}$	Clear, Set	25			ns	Figure 2	
t_s	Data Setup Time — HIGH	20			ns	Figure 1	
	LOW	20			ns		
t_h	Hold Time	5.0			ns	Figure 1	

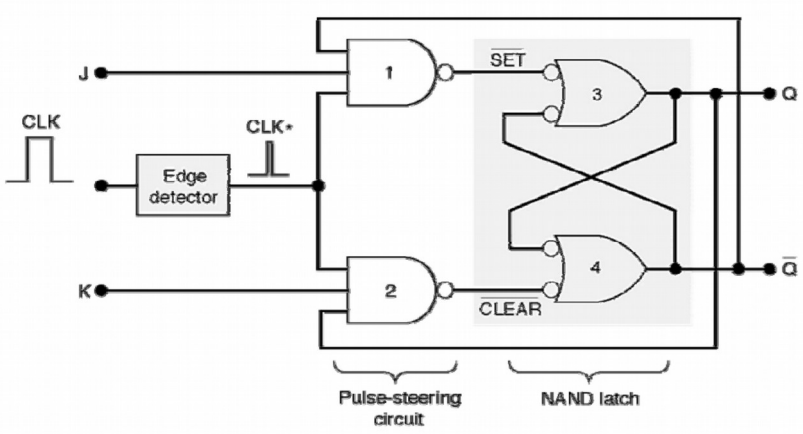
t_p = propagation delay;
t_s = setup time;
t_h = hold time;
t_w = assyncronous times.

Flip-Flop JK:

- Circuito interno



Flip-Flop JK:



MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

* Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H, h = HIGH Voltage Level

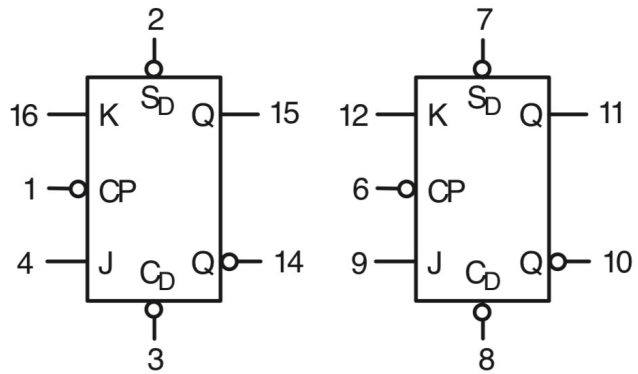
L, l = LOW Voltage Level

X = Immaterial

l, h (q) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the HIGH–to–LOW clock transition

Ex.: 74LS76:

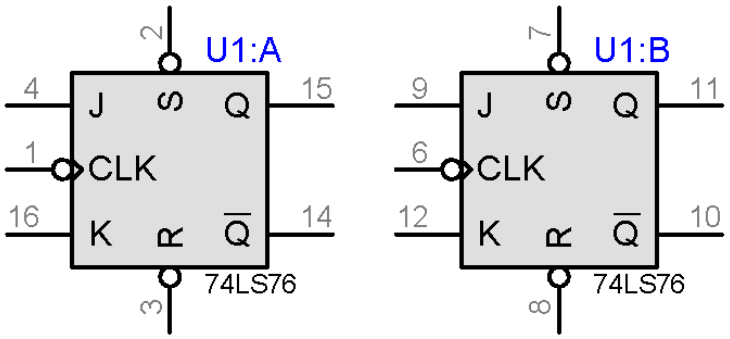
LOGIC SYMBOL

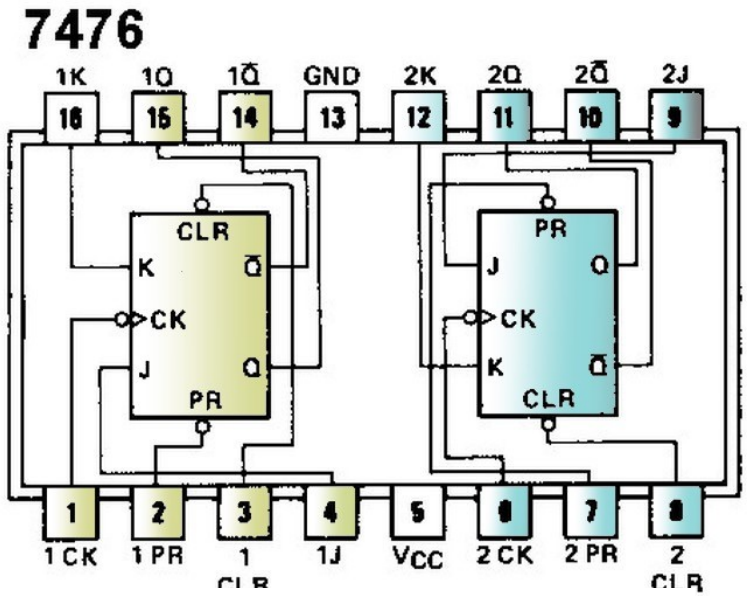


V_{CC} = PIN 5
GND = PIN 13

Dados: On Semiconductor (Division of Motorola; http://onsemi.com)

FF-JK: 74LS76





AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

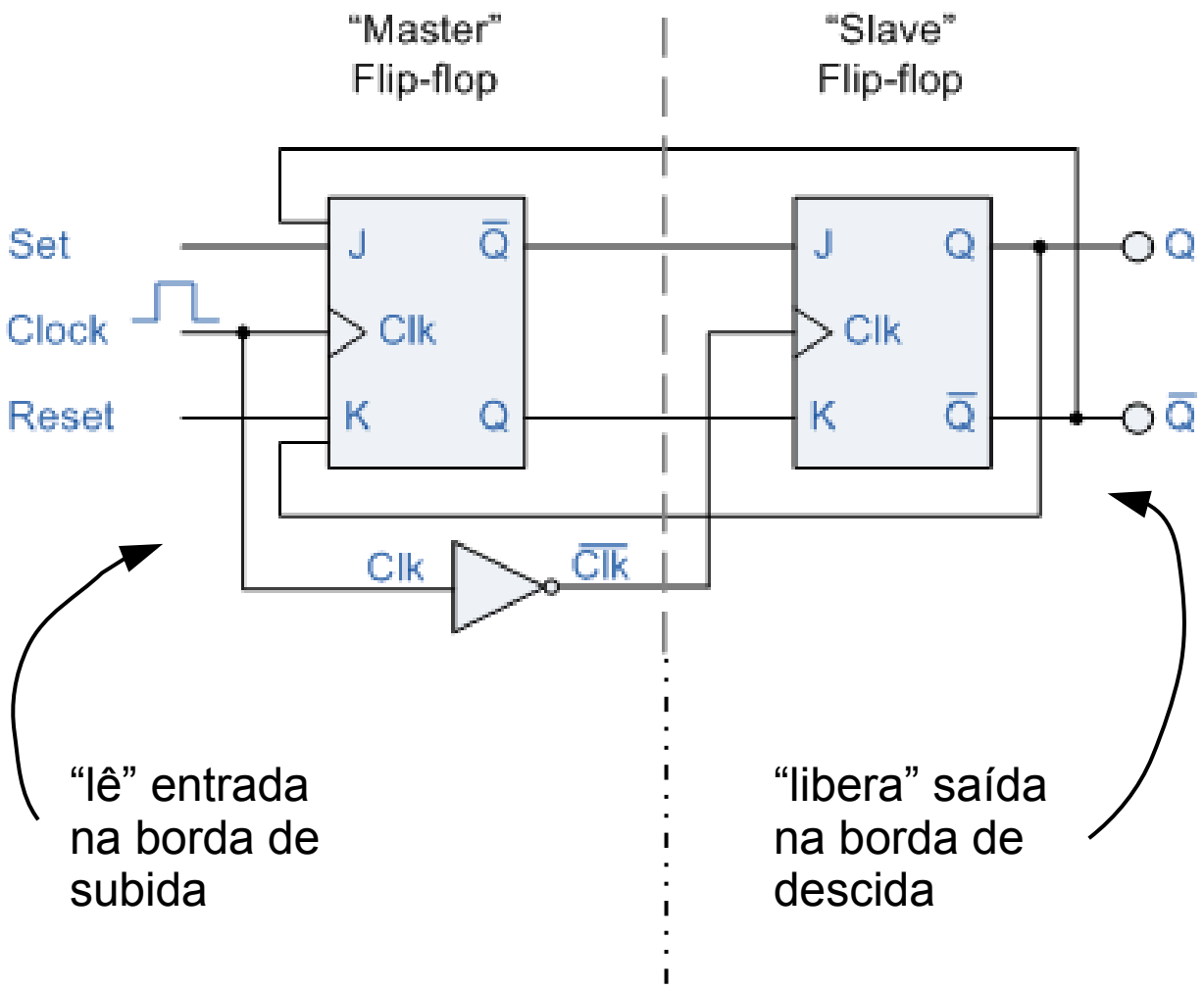
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	30	45		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Clock, Clear, Set to Output		15	20	ns	
			15	20	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

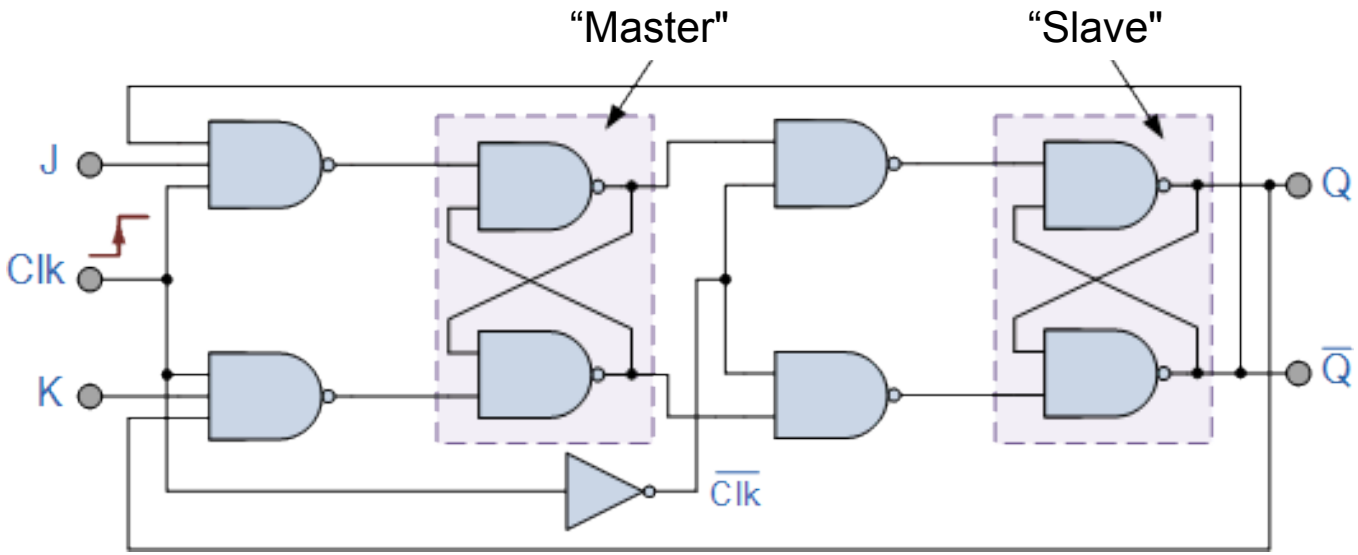
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Clock Pulse Width High	20			ns	V_{CC} = 5.0 V
t_W	Clear Set Pulse Width	25			ns	
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

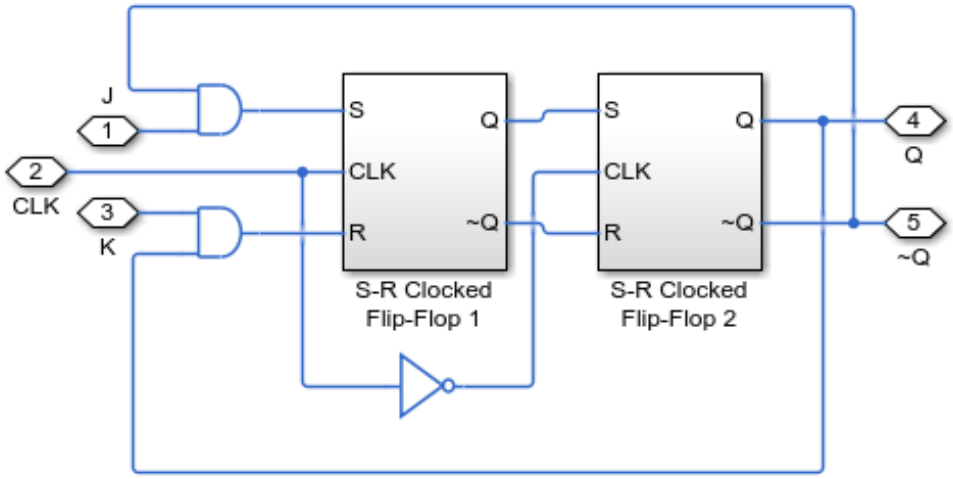

Biestáveis
Master-Slave...

FF RS MS (Master-Slave)



FF JK MS (Master Slave)





Atenção: 74LS76 ≠ 7476!

SN74LS76A

Dual JK Flip-Flop with Set and Clear

The SN74LS76A offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW clock transitions.

'LS76A FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

FAIRCHILD SEMICONDUCTOR™

September 1986
Revised July 2001

DM7476

Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs

'76 FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	⊓	L	L	Q_0	$\overline{Q}_0$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	