# Registradores de Deslocamento

## Shift Registers

Prof. Fernando Passold

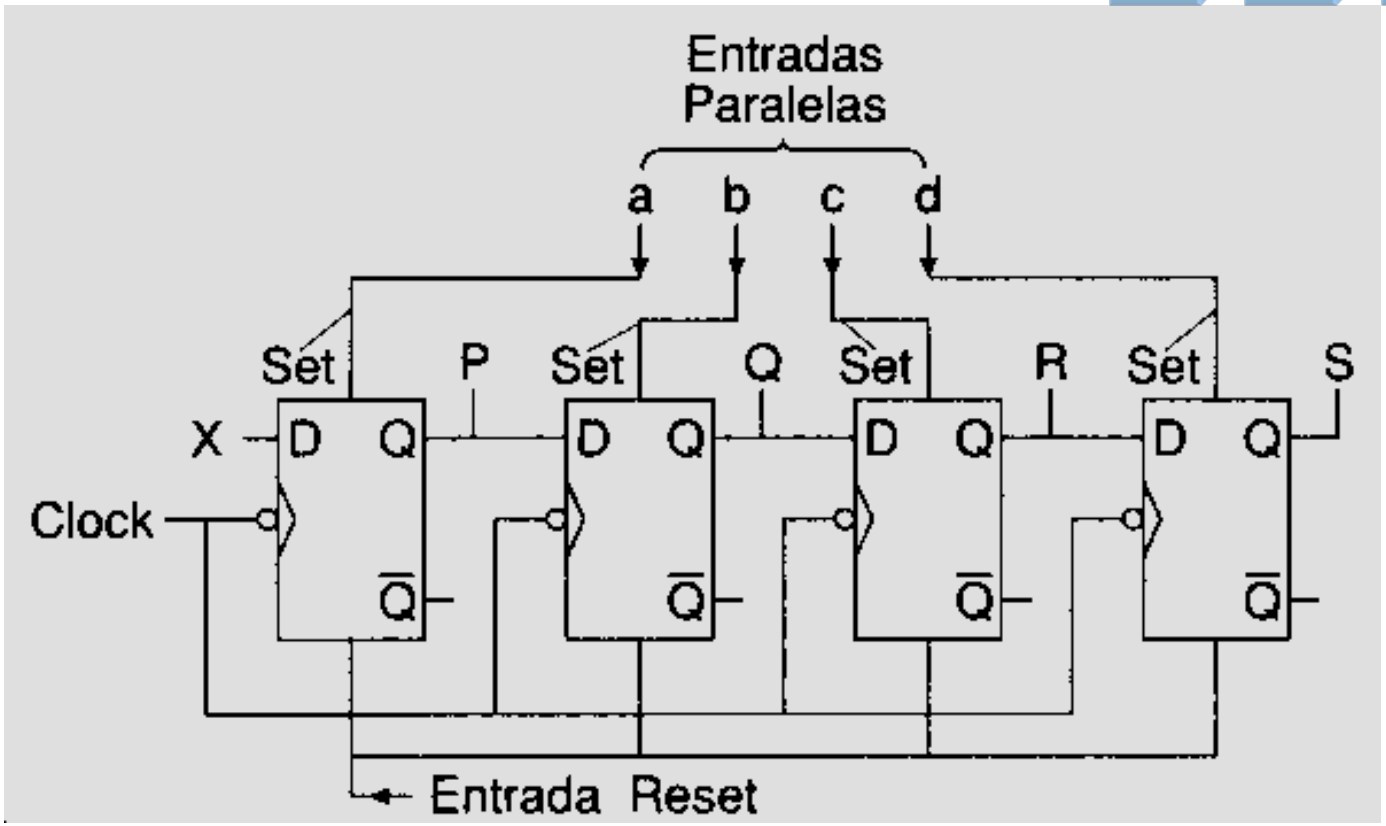
Set/2016... Nov/2008 (UCV)

# Introdução

- O que acontece quando se cascateia FFs de maneira síncrona?
  - Podem ocorrer 3 coisas:
    - Se obtêm um contador síncrono;
    - Se obtêm um contador especial;
    - Se obtêm um registrador de deslocamento.

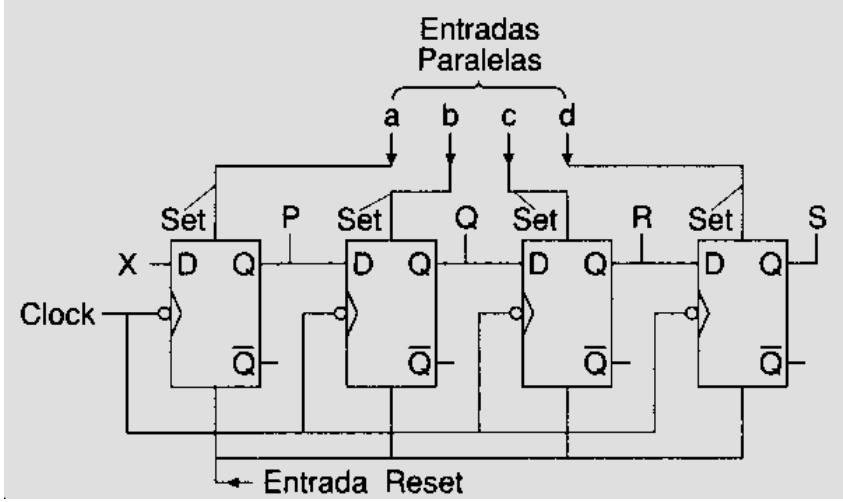
# Introdução

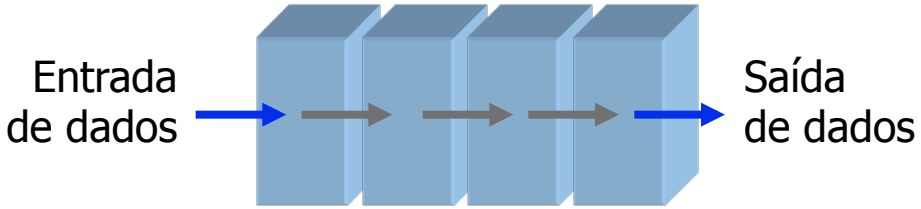
- O que acontece quando se cascateis FFs de maneira síncrona ?
  - Podem ocorrer 3 coisas:
    - Se obtêm um contador síncrono;
    - Se obtêm um contador especial;
    - Se obtêm um registrador de deslocamento:



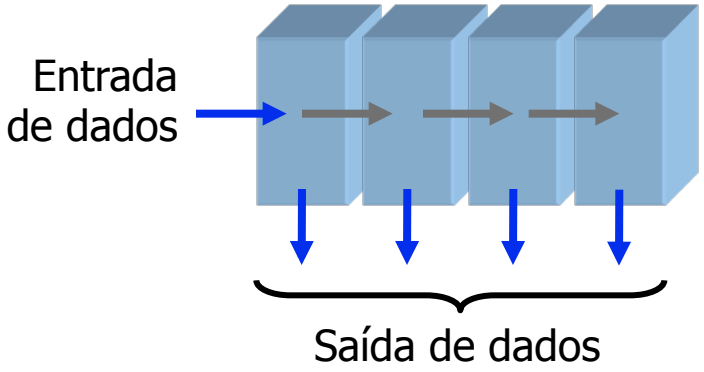
# Introdução

- Operações típicas de registradores de deslocamento, exemplos:

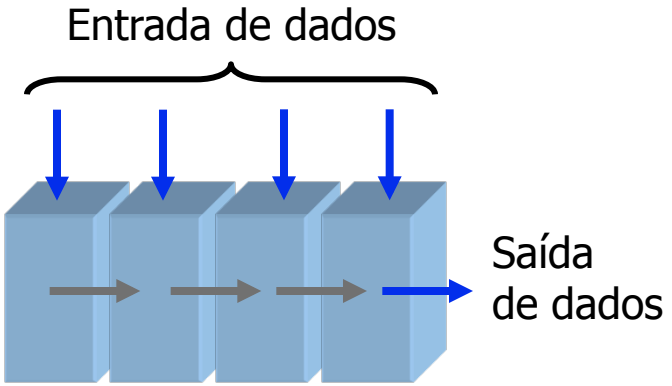



(a) Registrador de entrada série e saída série com deslocamento para direita.
(Serial-in, Serial-out)



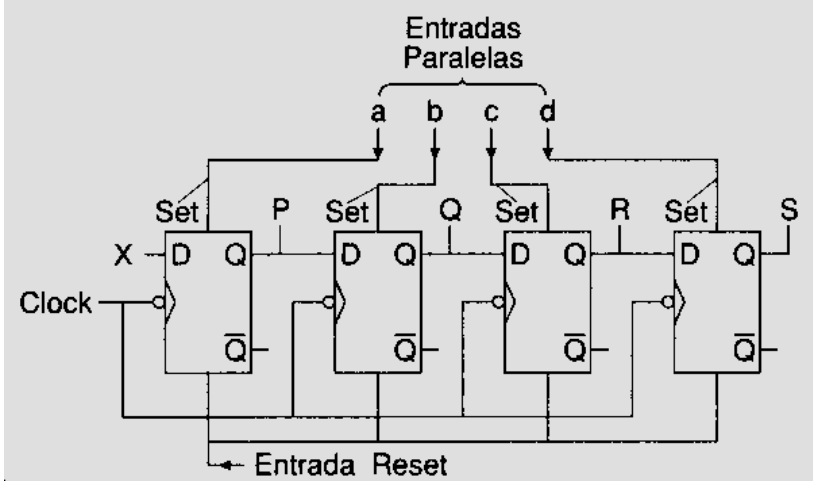

(b) Registrador de entrada série e saída paralela com deslocamento para direita.
(Serial-in, Parallel-out)

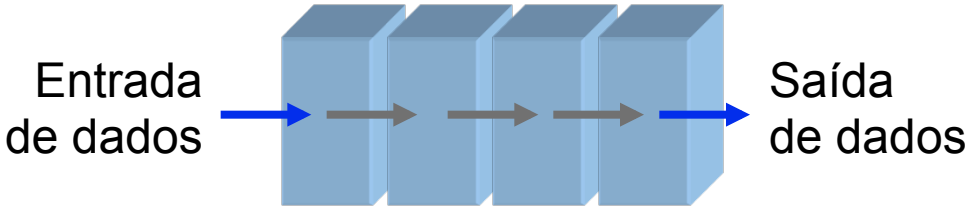



(c) Registrador de entrada paralela e saída série com deslocametno para direita
(Parallel-in, Serial-out, Shift right Register).

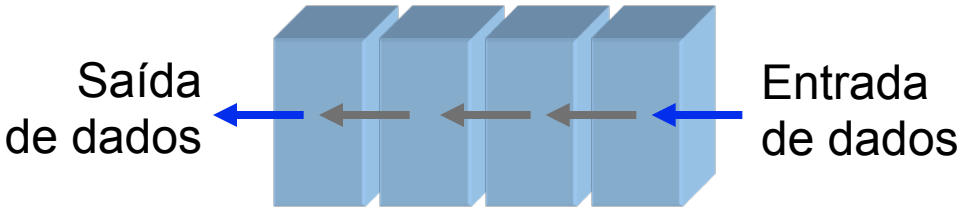
# Introdução

- Operações típicas de registradores de deslocamento, exemplos:

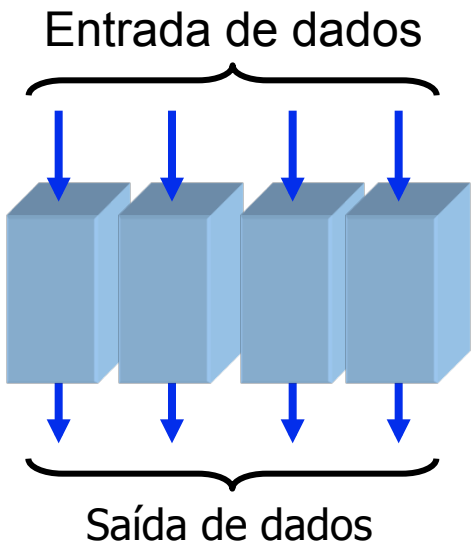



(a.1) Registrador de entrada série e saída série com deslocamento para **direita**.
(shift right register)



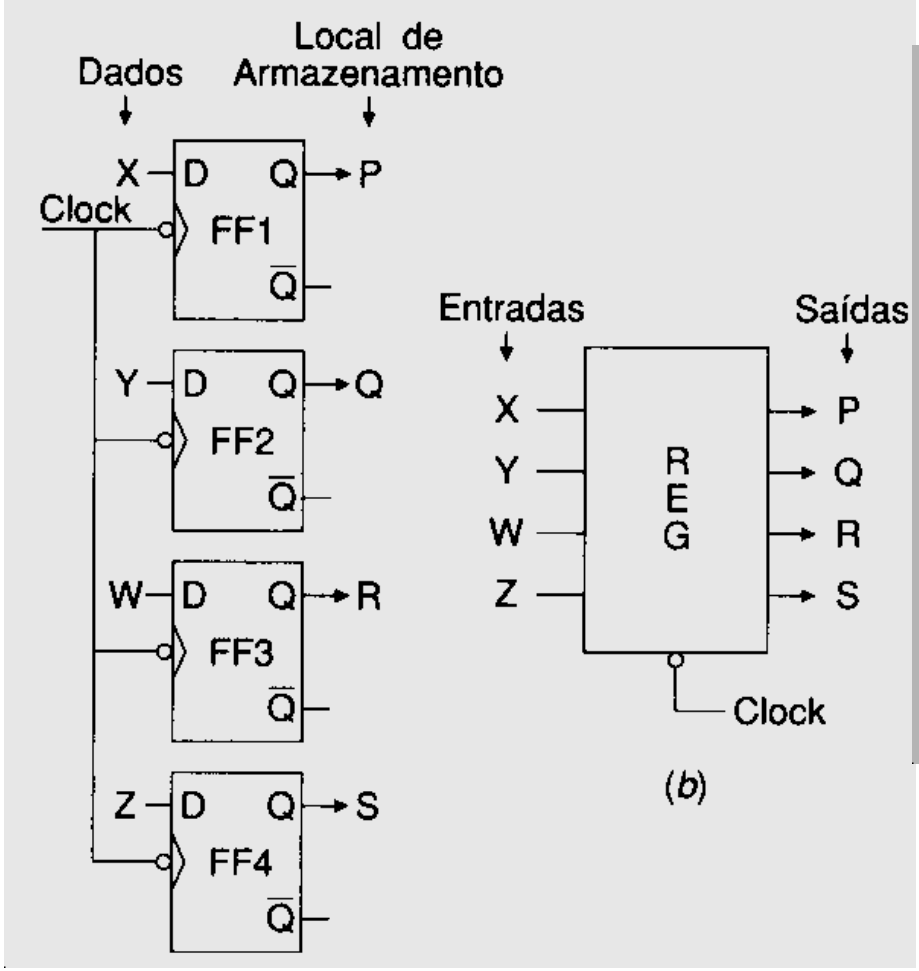

(a.2) Registrador de entrada série e saída série com deslocamento para **esquerda**.
(shift left register)



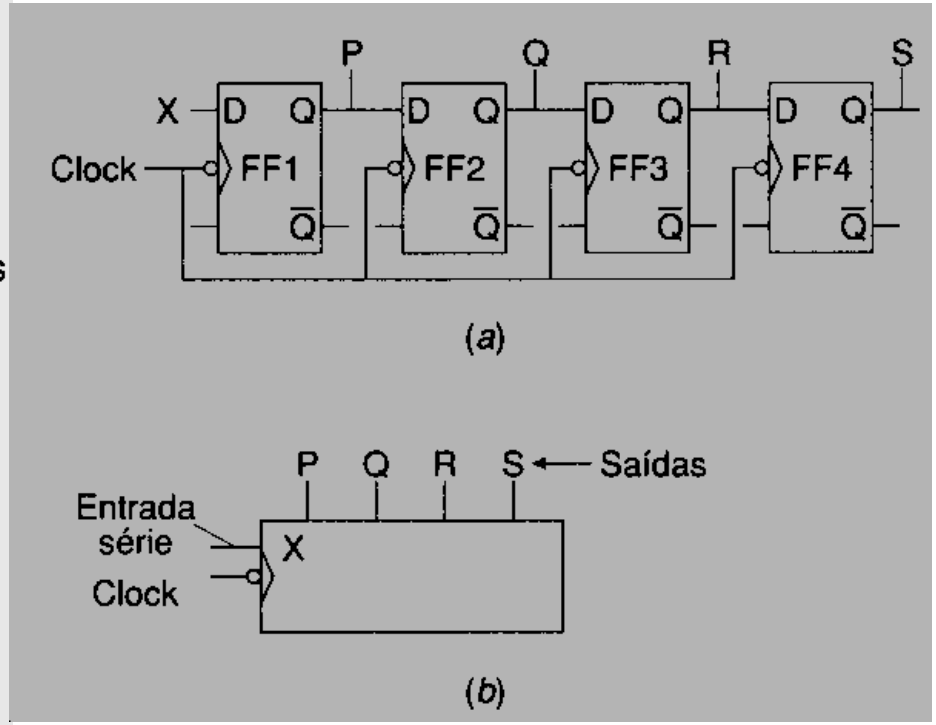

(d) Registrador de entrada paralela e saíra paralela.
(Parallel-in, Parallel-out)

# Tipos de Registradores:

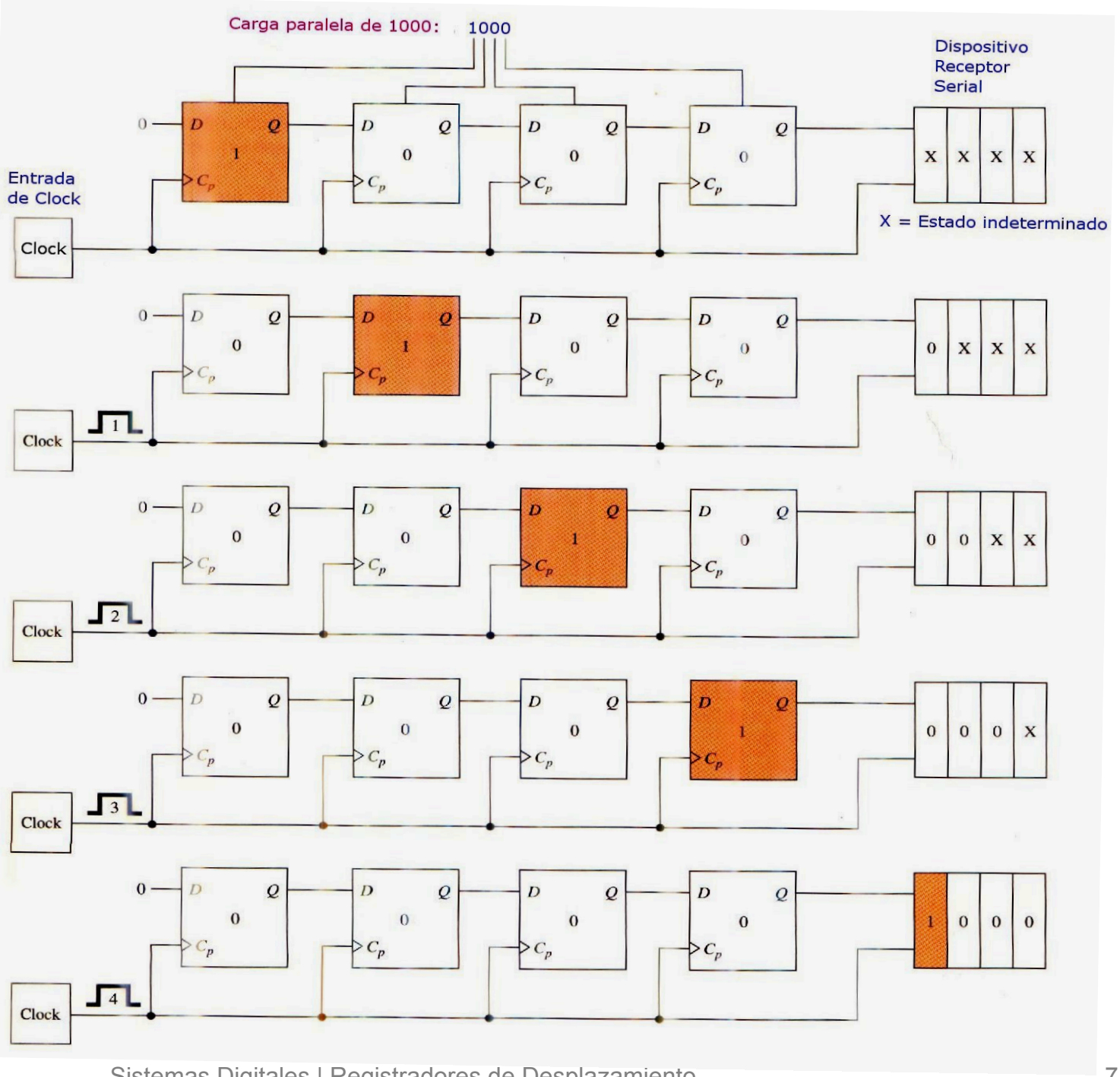
- **Caso de Registrador paralelo**



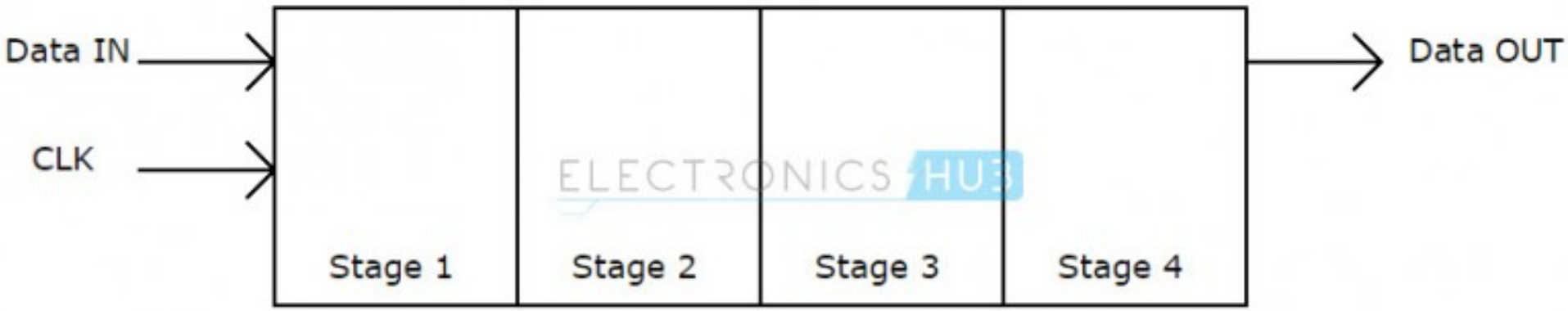

- **Caso de Registrador Série:**



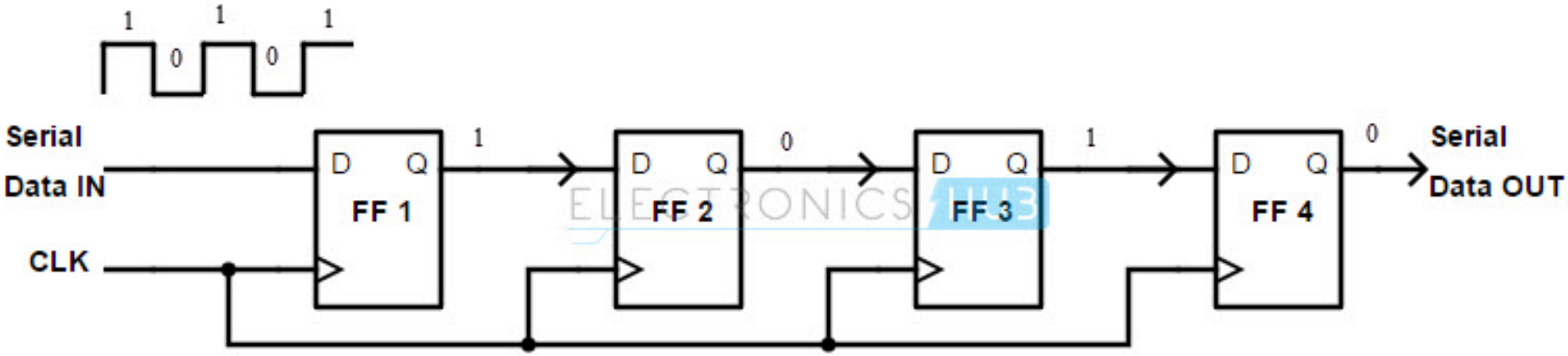
# Exemplo de conversão paralelo → serial usando registrador de 4 bits



# Registrador de entrada Serial, saída Serial




Shift right registers



# Registrador de Entrada Paralela (EP) / Saída Serie (SS):

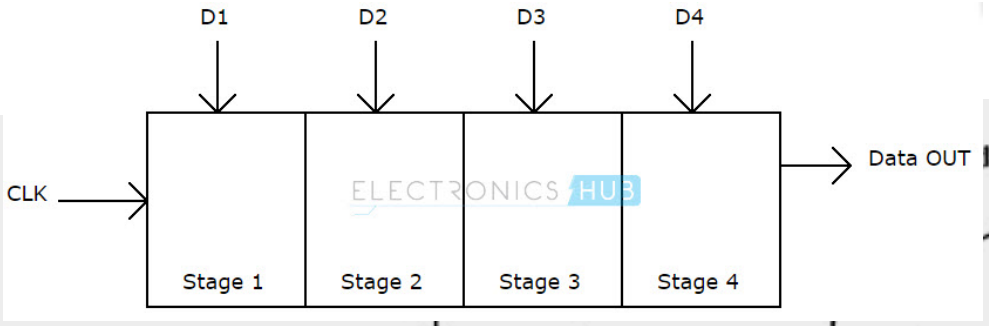
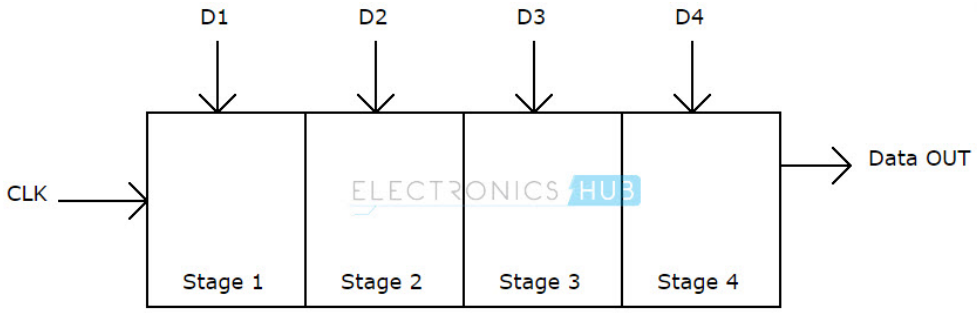


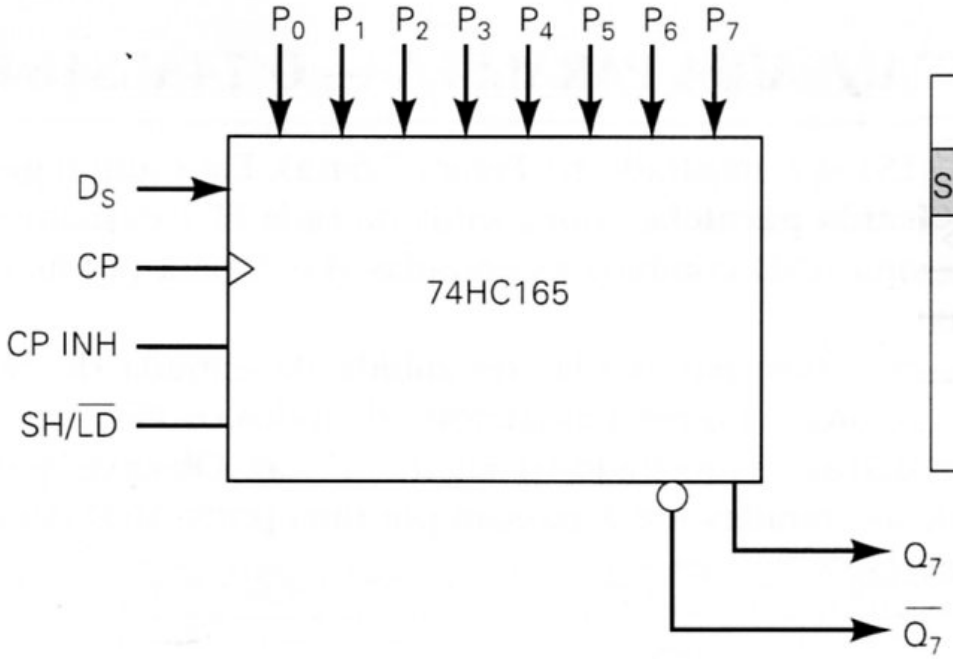




Figura 8.7 . *Registrador de deslocamento EP/SS .*

# Registrador de Entrada Paralela (EP) / Saída Serie (SS):




| Entradas | | | Operação |
|---|---|---|---|
| SH/$\overline{LD}$ | CP | CP INH | |
| L | X | X | Carga paralela |
| H | H | X | Não muda |
| H | X | H | Não muda |
| H | ↓ | L | Deslocamento |
| H | L | ↓ | Deslocamento |

H = nível alto
L = nível baixo
X = irrelevante
↓ = PGT

# Registrador de Entrada Paralela/Saída Paralela (EP/SP):

- Ex_2) circuito comercial: 74**174** **(Parallel In / Parallel Out):**

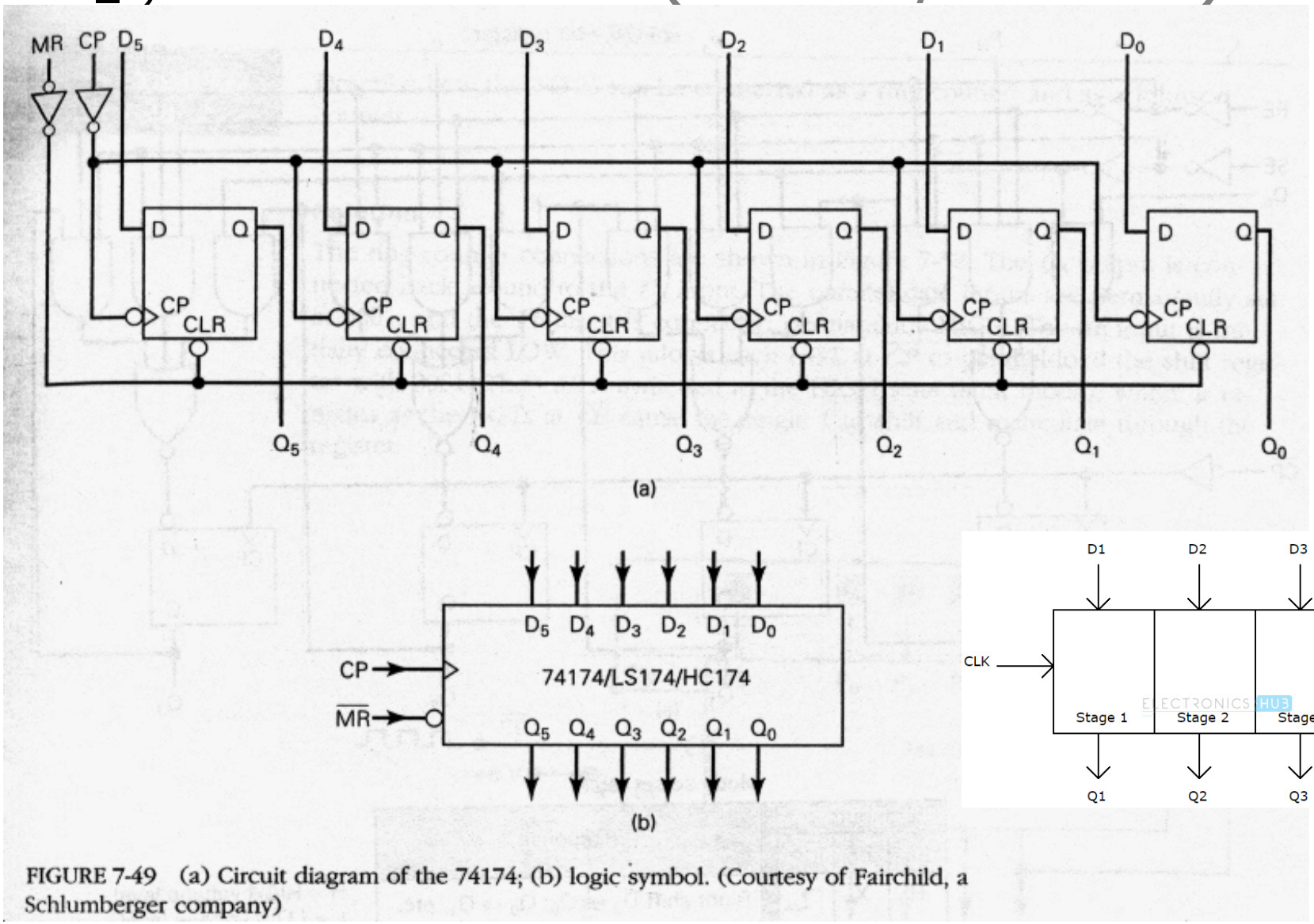


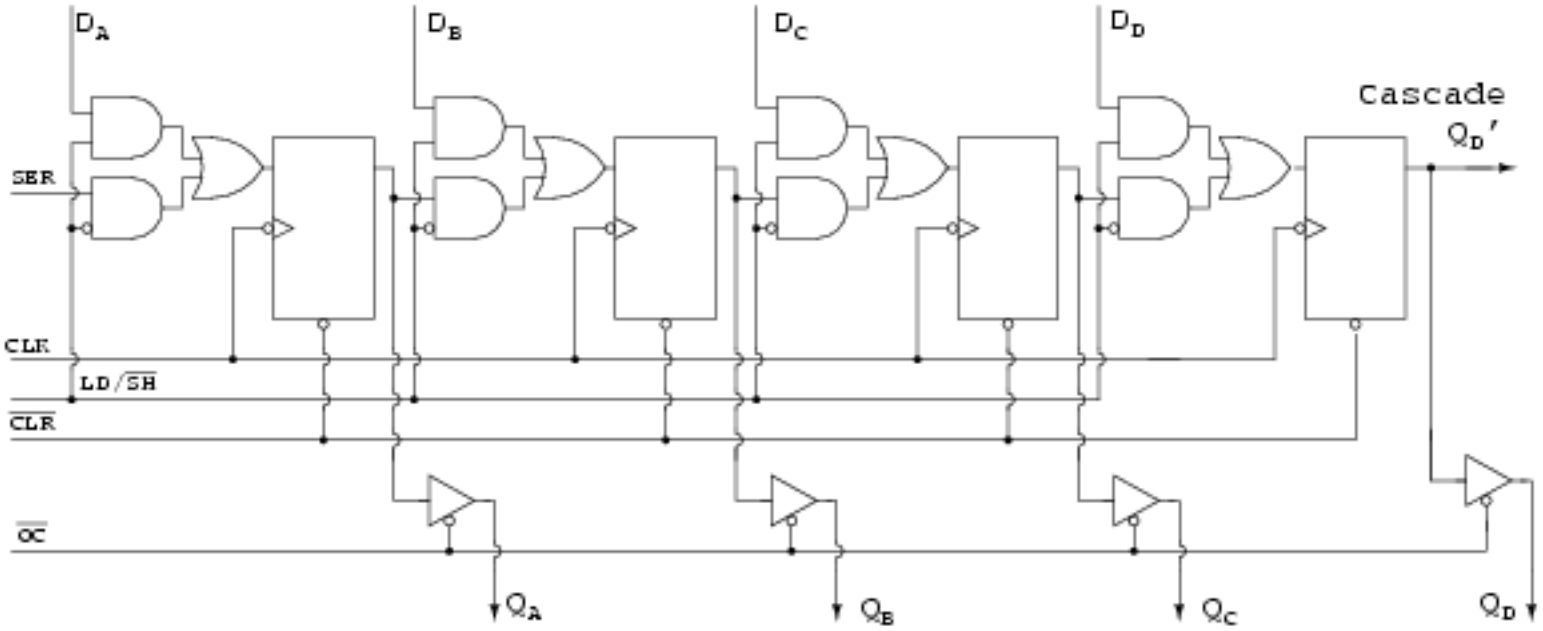




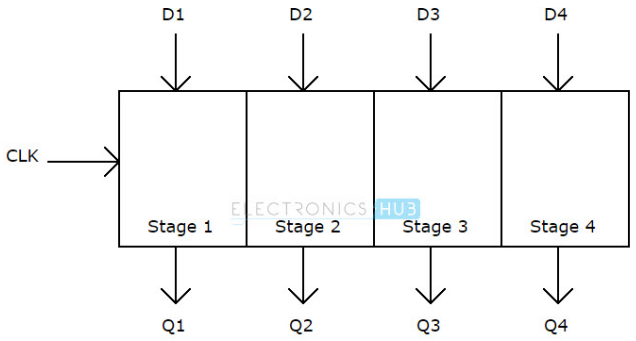
FIGURE 7-49 (a) Circuit diagram of the 74174; (b) logic symbol. (Courtesy of Fairchild, a Schlumberger company)

# Registrador de Entrada Paralela/Saída Paralela (EP/SP):

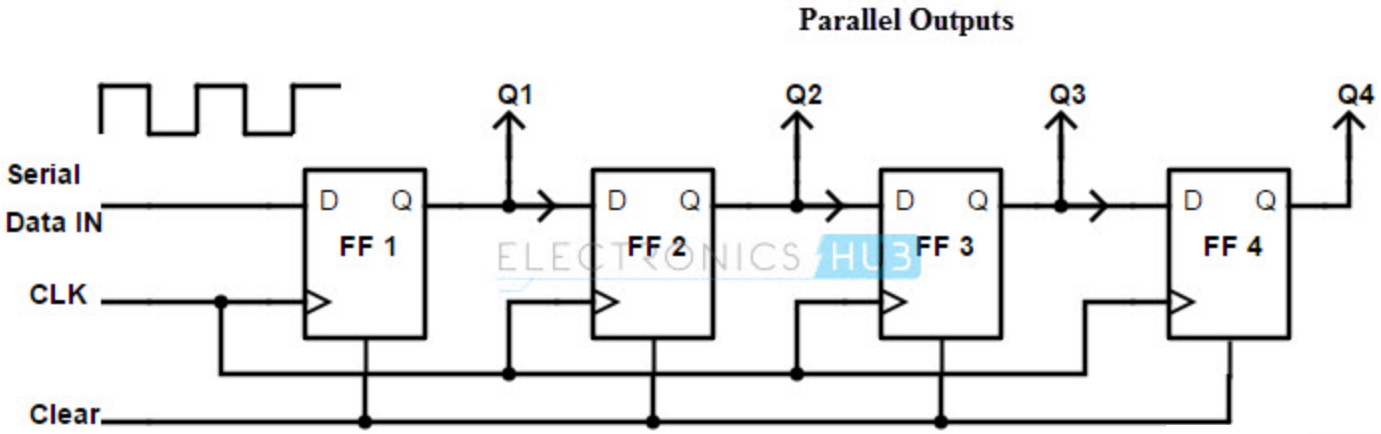
- Ex_3) circuito comercial: 74LS395

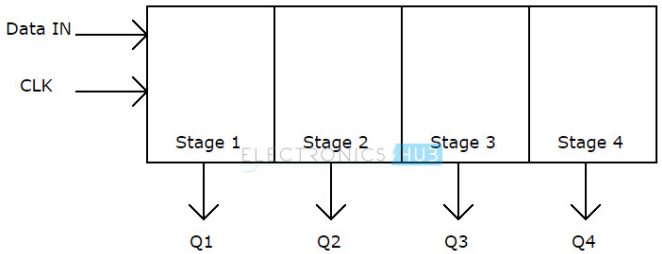



74LS395 parallel-in/ parallel-out shift register with tri-state output

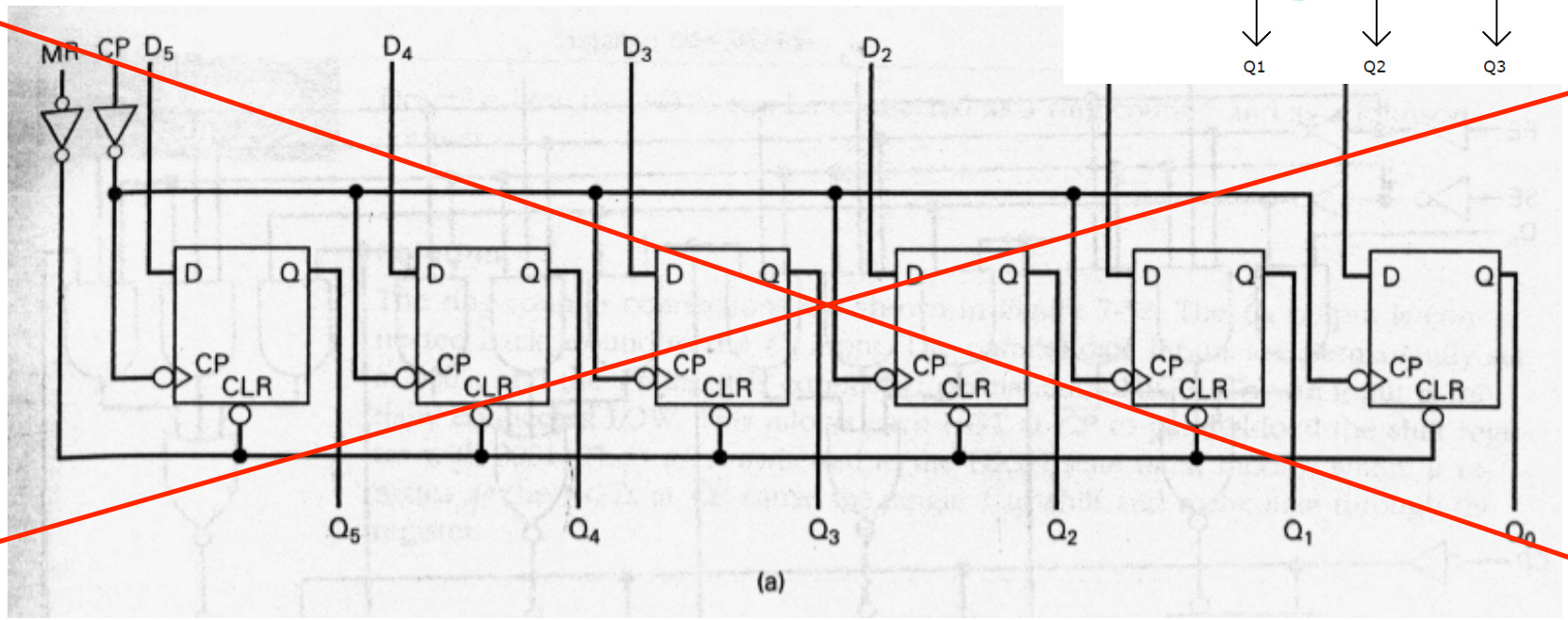


# Registrador de Entrada Série/Saída Paralela (ES/SP):



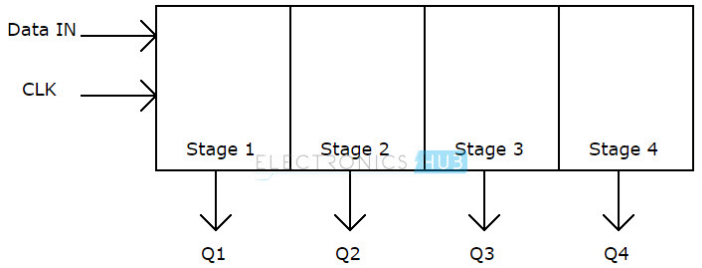




- Ejemplo: CI 74**164**
  (Registrador de Entrada Serial / Saída Paralela, de 8 bits)



# Registrador de Entrada Série/Saída Paralela (ES/SP):

- Ejemplo: CI 74**164** (Registrador de Entrada Serial / Saída Paralela, de 8 bits)



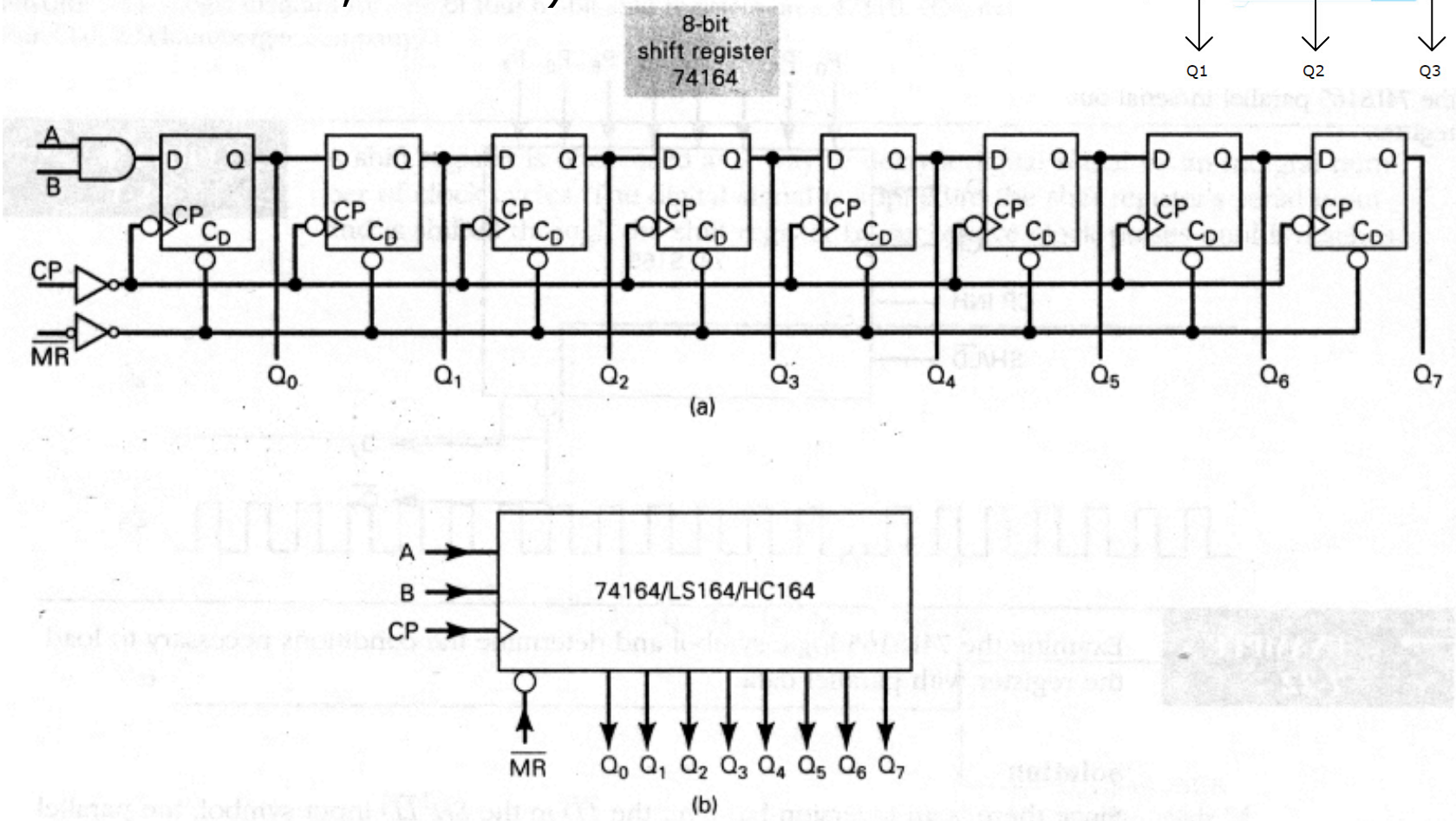




FIGURE 7-56 (a) Logic diagram for the 74164; (b) logic symbol. (Courtesy of Fairchild, a Schlumberger company)

# Registrador de Entrada Série/Saída Paralela (ES/SP):

- Exemplo de uso de CI 74**164**
  (Registrador de Entrada Serial / Saída Paralela, de 8 bits)

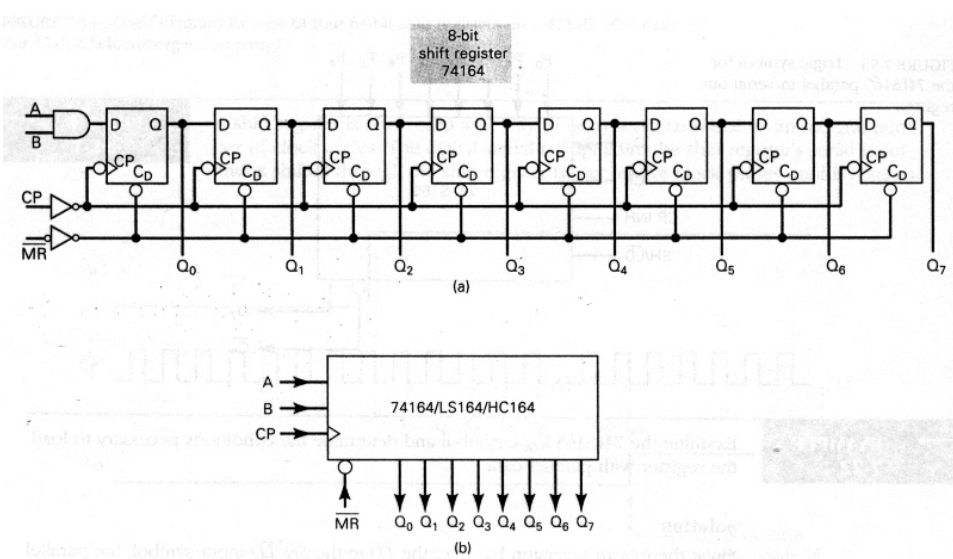
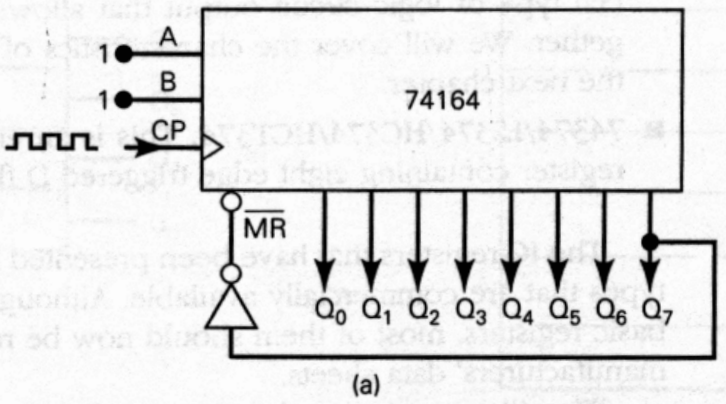



FIGURE 7-56 (a) Logic diagram for the 74164; (b) logic symbol. (Courtesy of Fairchild, a Schlumberger company)

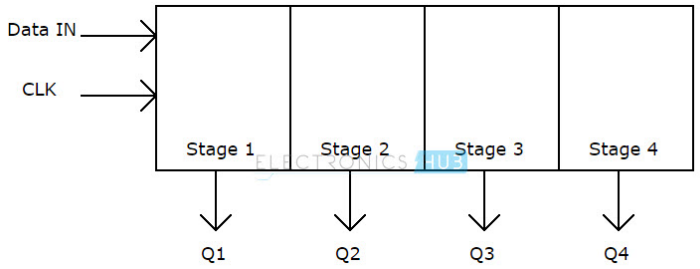



| ber | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 4 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 5 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 7 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Recycles

Temporary state

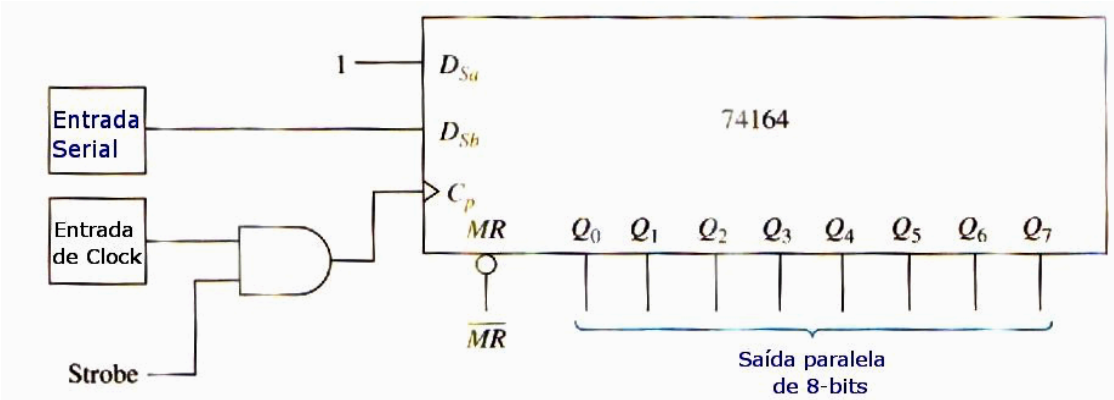
(b)



# Aplicações:

***Exemplo:***

- Circuito de conversão serial para paralelo do número binário 11010010 usando o registrador de deslocamento 74164:

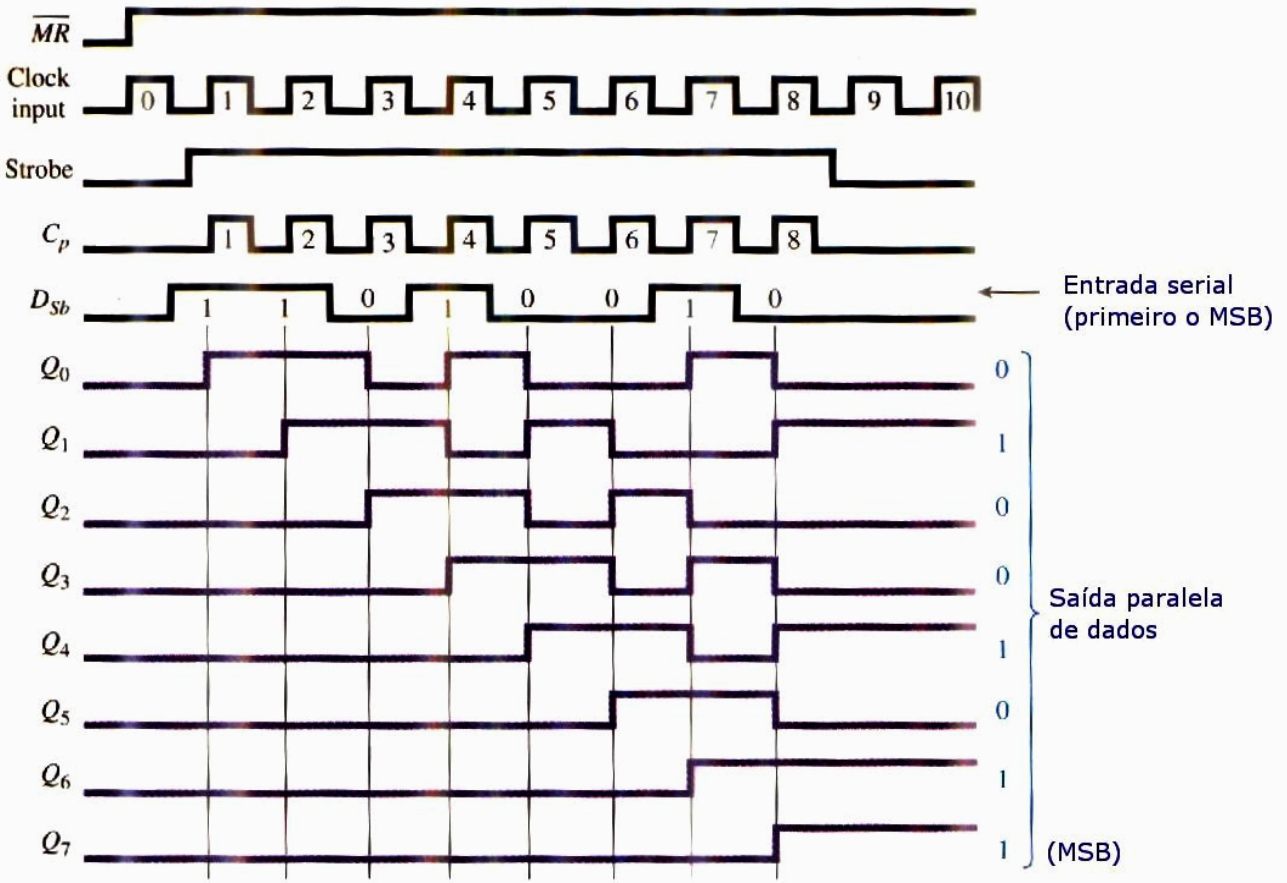



1) O registrador é "limpo" (recebe um signal de Clear o Reset) → suas saídas, $Q_0$-$Q_7$ vão para nivel lógico baixo;

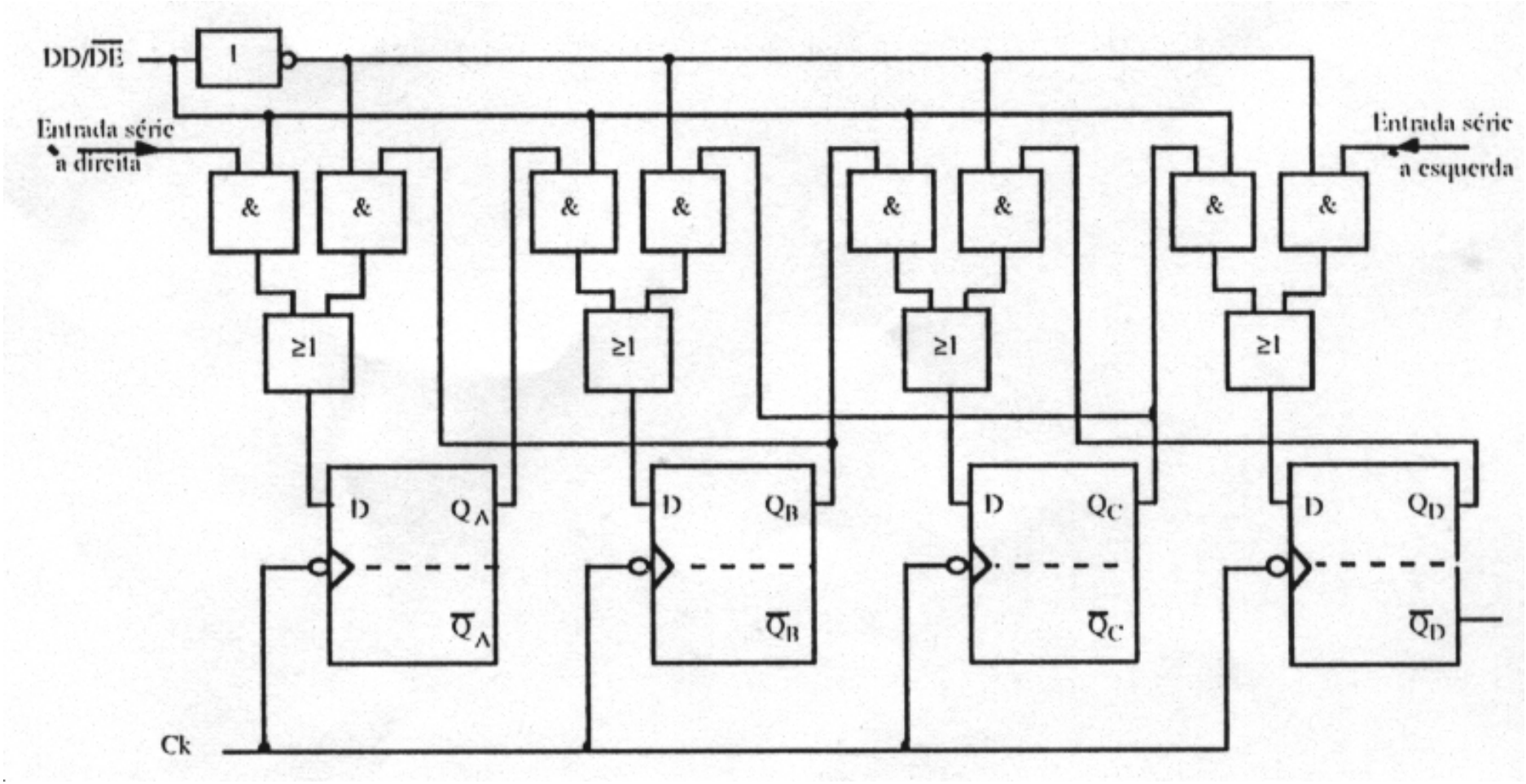
2) O sinal "**Strobe**" é necessário para garantir que somente 8 pulsos de clock ingressem no circuito;

3) Os dados seriais ingressam na linha $D_{Sb}$, sendo que o primeiro bit é o MSB;

4) Depois de 8 pulsos de clock, os 8 bits de datos podem ser lidos nos pinos de saídas paralelas de dados (el bit MSB vai estar em $Q_7$ e o LSB em $Q_0$).

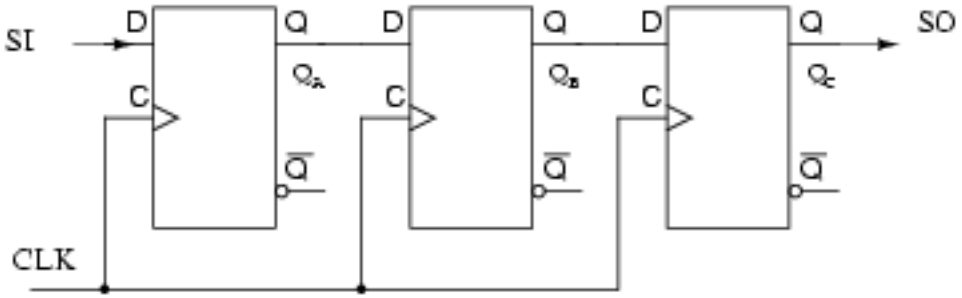


# Registrador Bidirecional:
## Bidirectional Shift Register:



# Registrador Bidirecional:
## Bidirectional Shift Register:

Shift right:



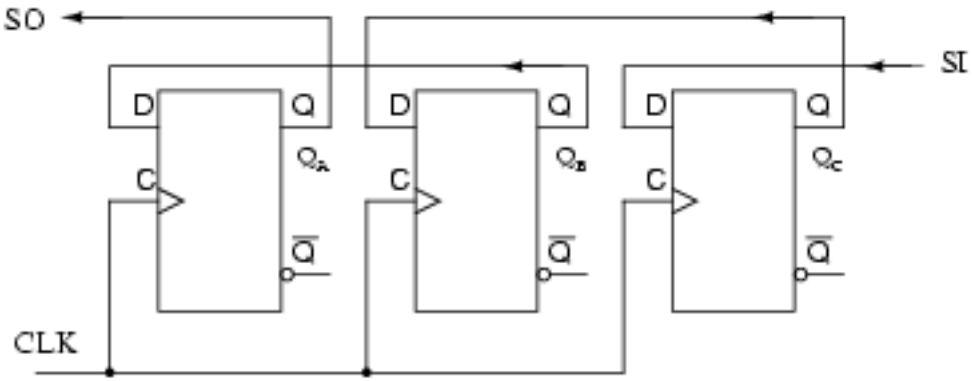

Shift right

| | $Q_A$ | $Q_B$ | $Q_C$ |
|---|---|---|---|
| load | 1 | 1 | 0 |
| shift | X | 1 | 1 |

→

Load and right shift

Shift left:



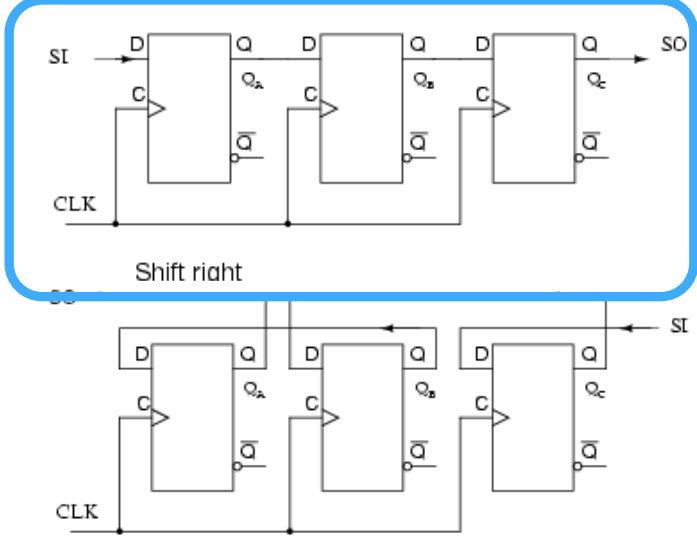

Shift left

| | $Q_A$ | $Q_B$ | $Q_C$ |
|---|---|---|---|
| load | 1 | 1 | 0 |
| shift | 1 | 0 | X |

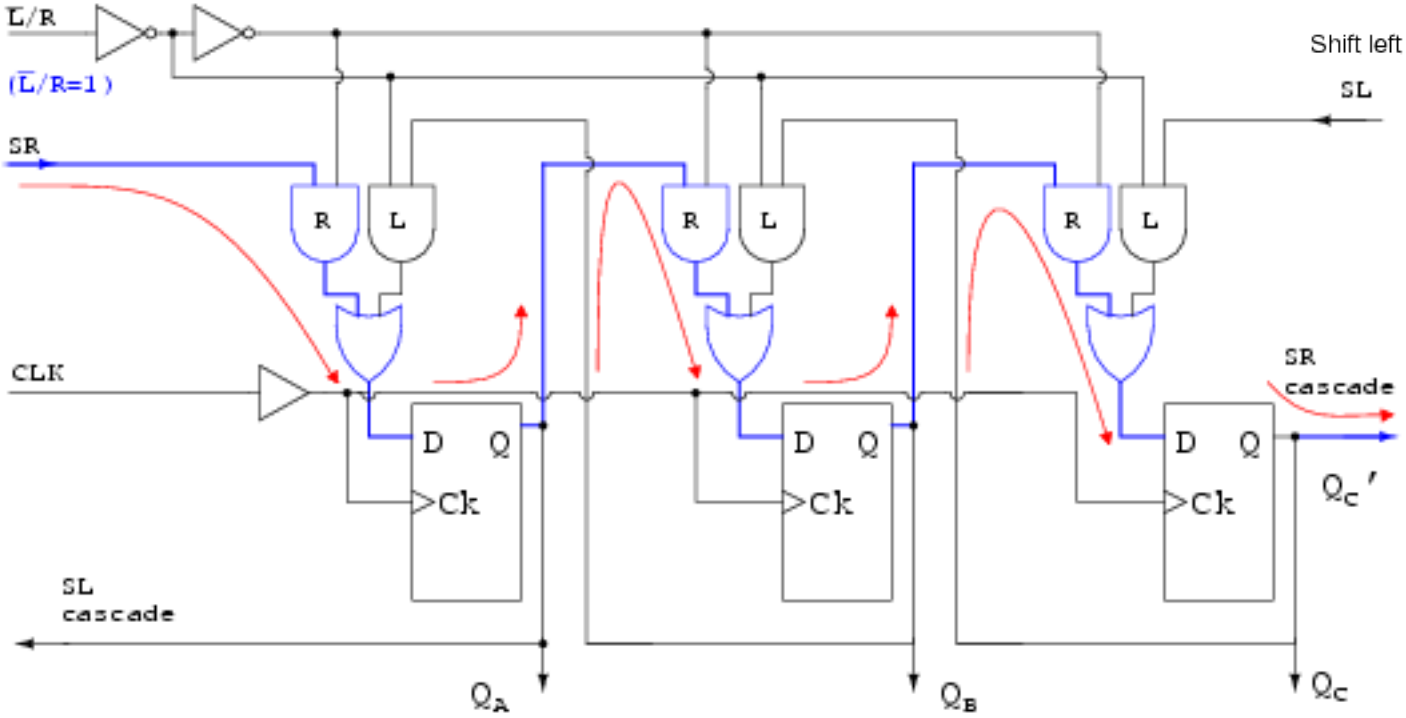
←

Load and left shift

# Registrador Bidirecional:

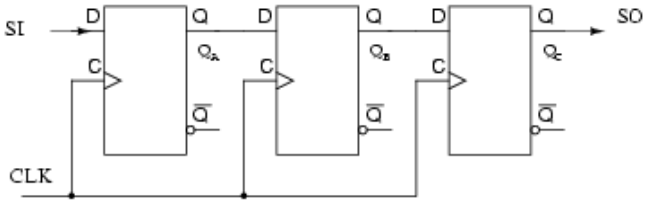


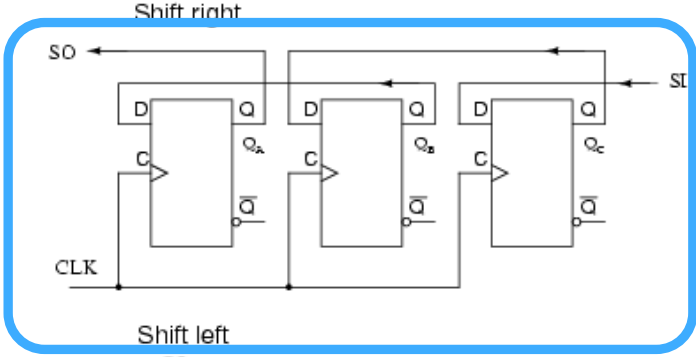

Registrador biderecional/deslocamento para direita:



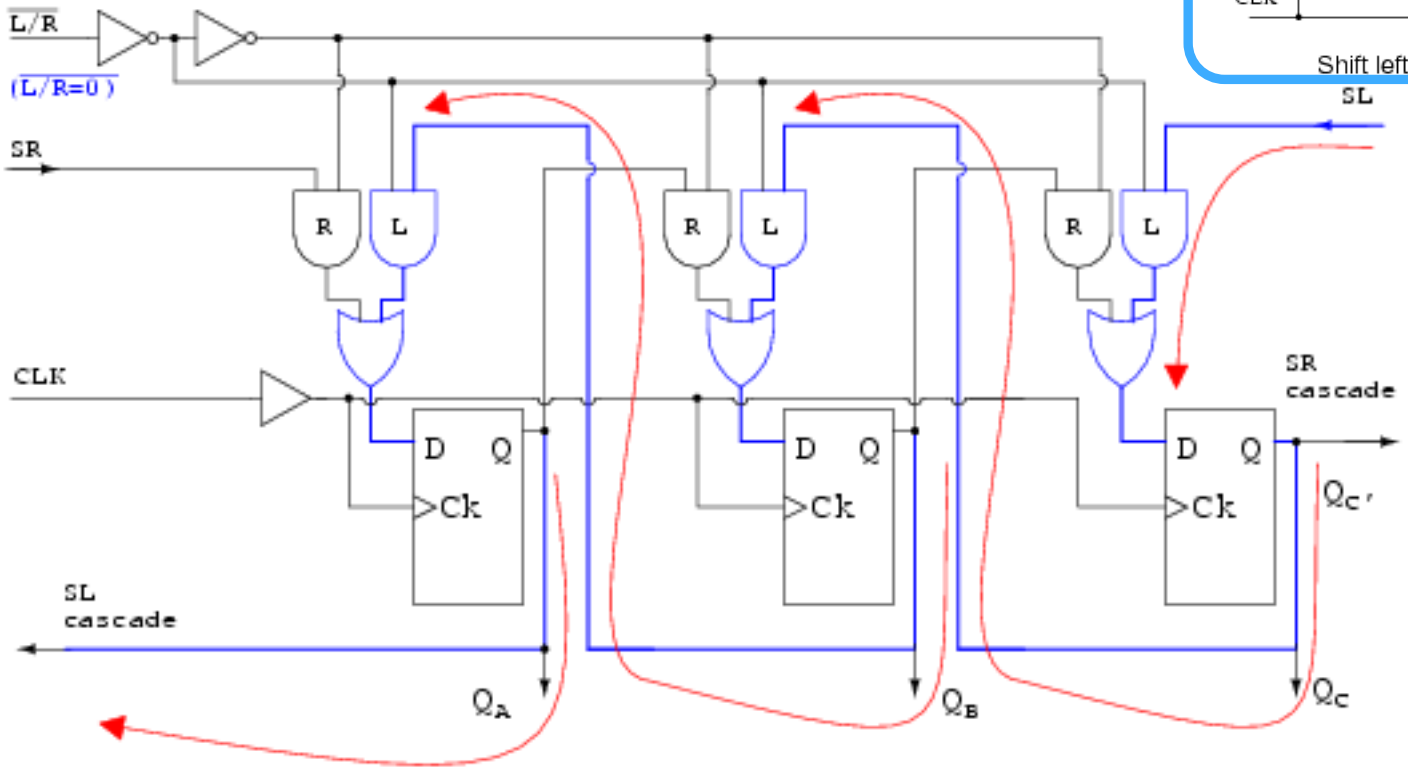

Shift left/ right, right action

# Registrador Bidirecional:



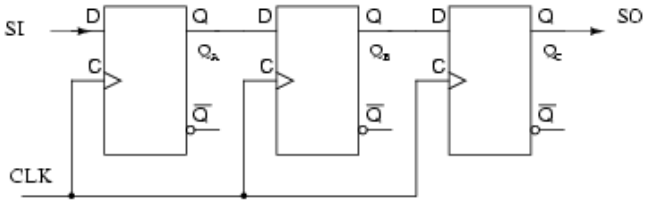




Registrador biderecional/deslocamento para esquerda:

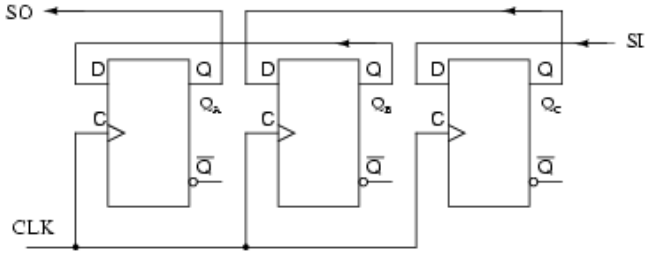



Shift left/ right register, left action

# Registrador Bidirecional:

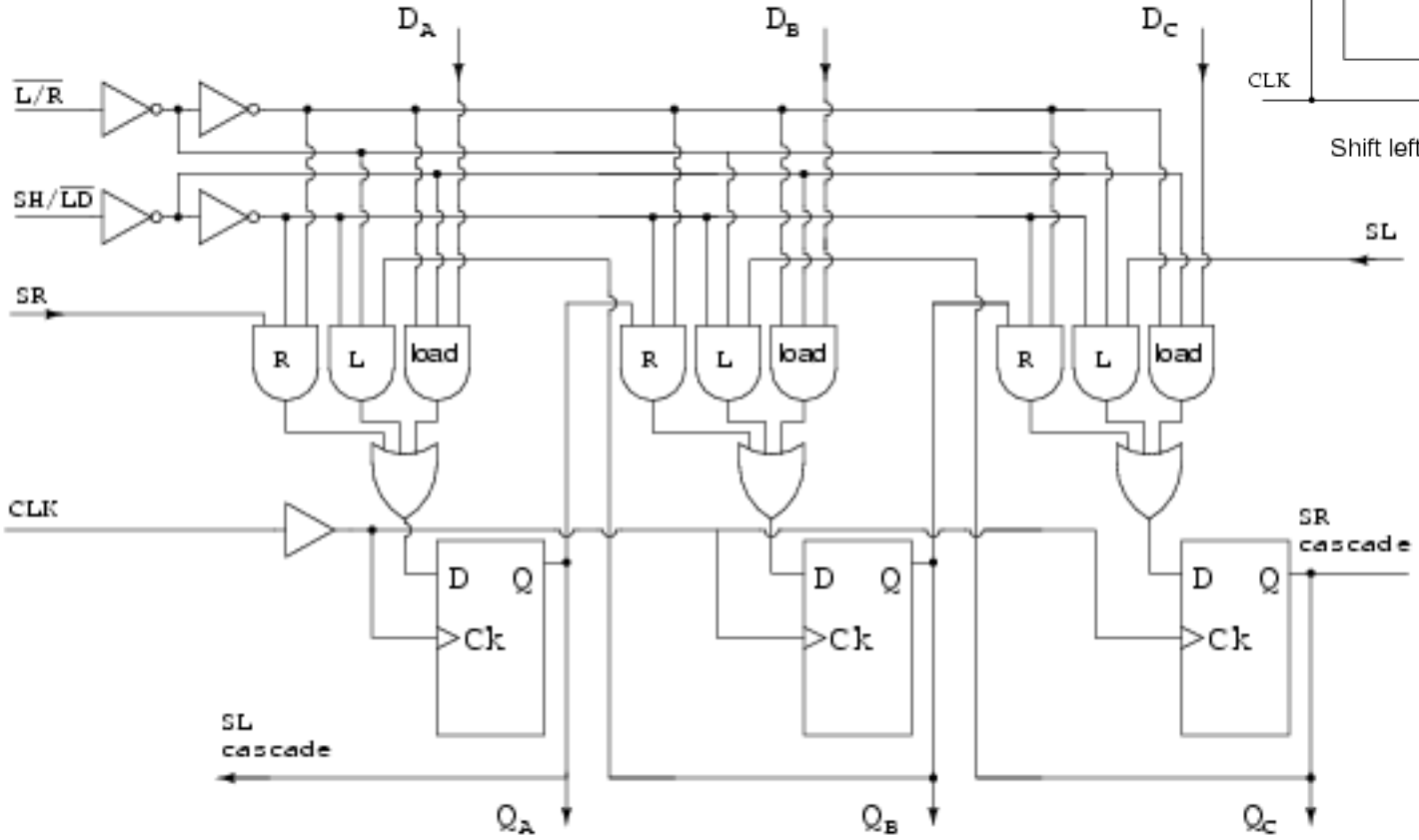



Shift right




Shift left

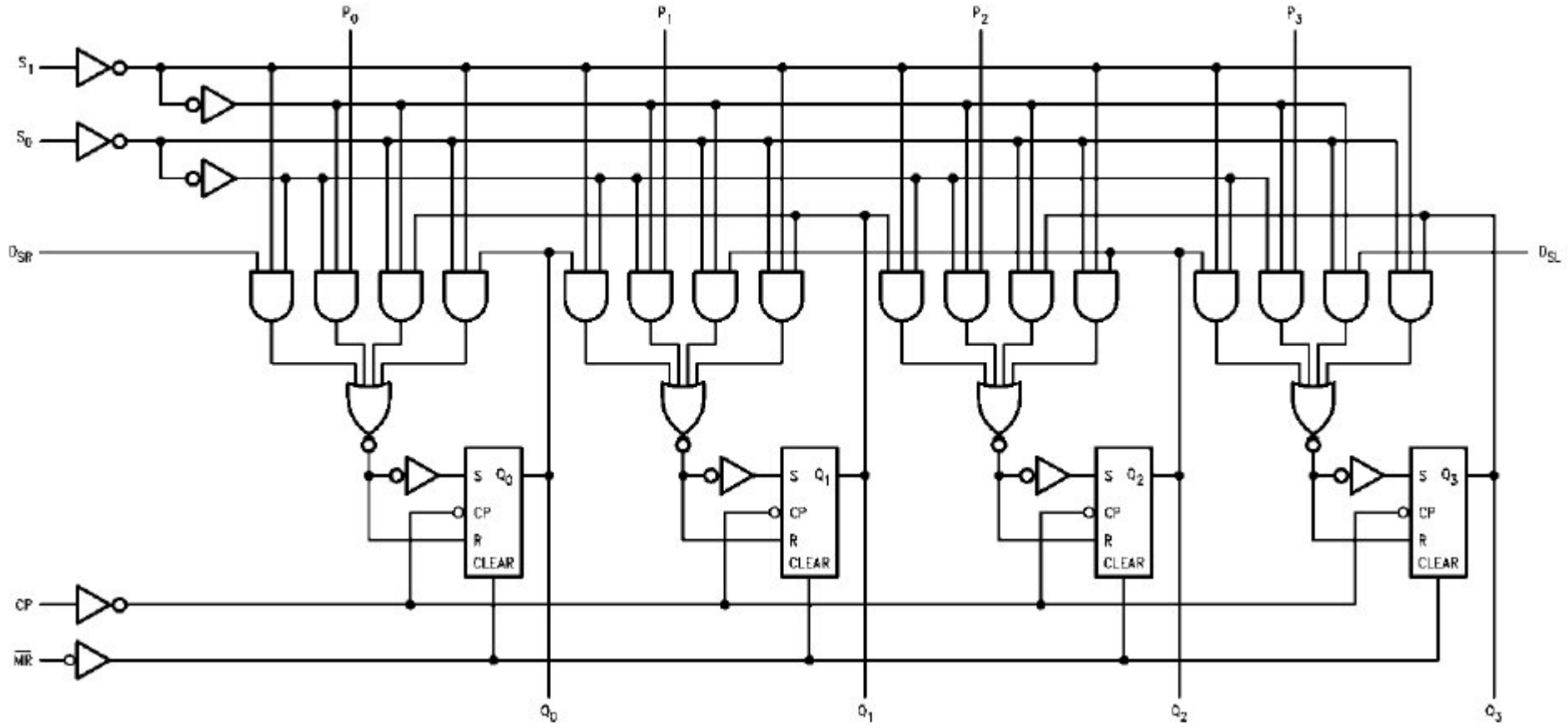
Registrador bidirecional/circuito completo:




Shift left/ right/ load

# Registrador Bidirecional:
## Bidirectional Shift Register:

- Exemplo comercial: CI 74194

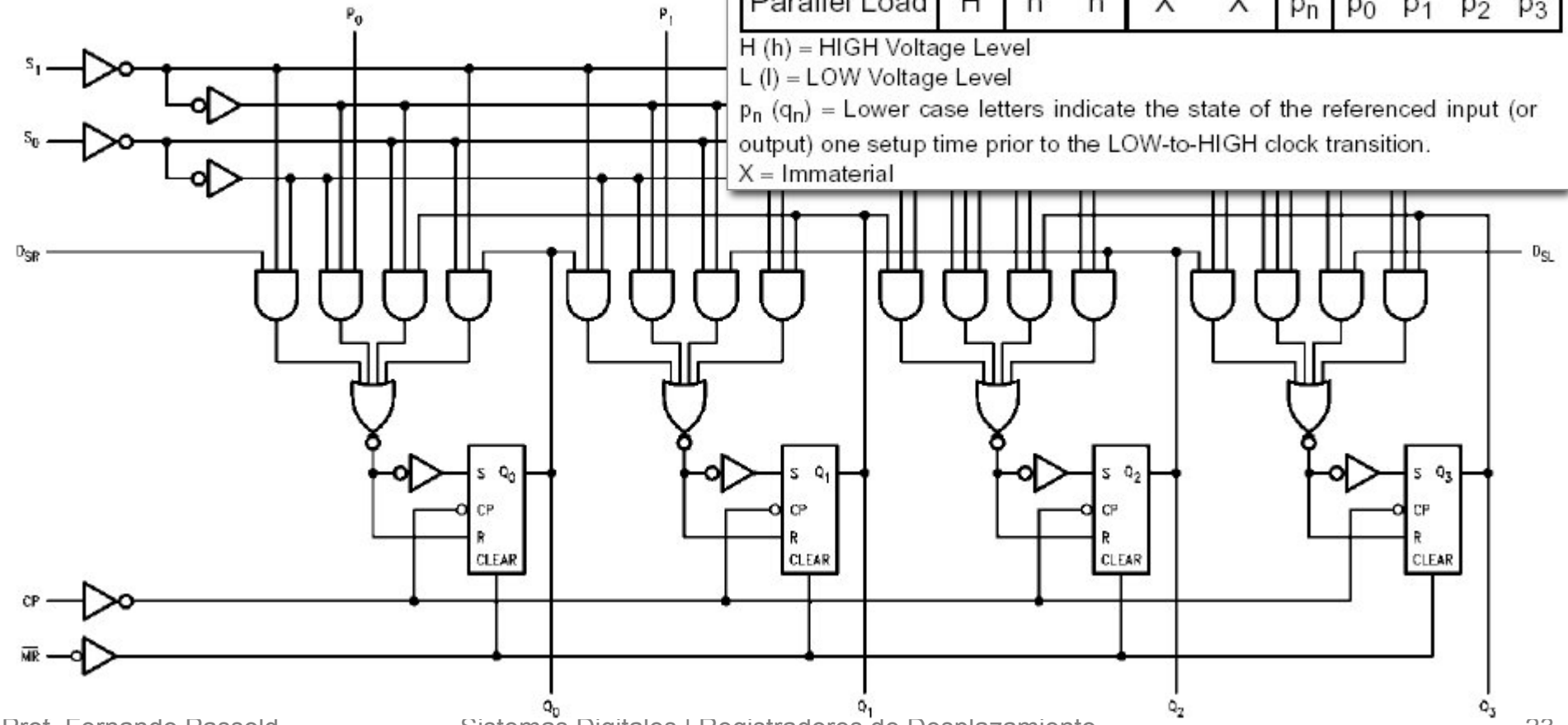


# Registrador bidireccional Universal

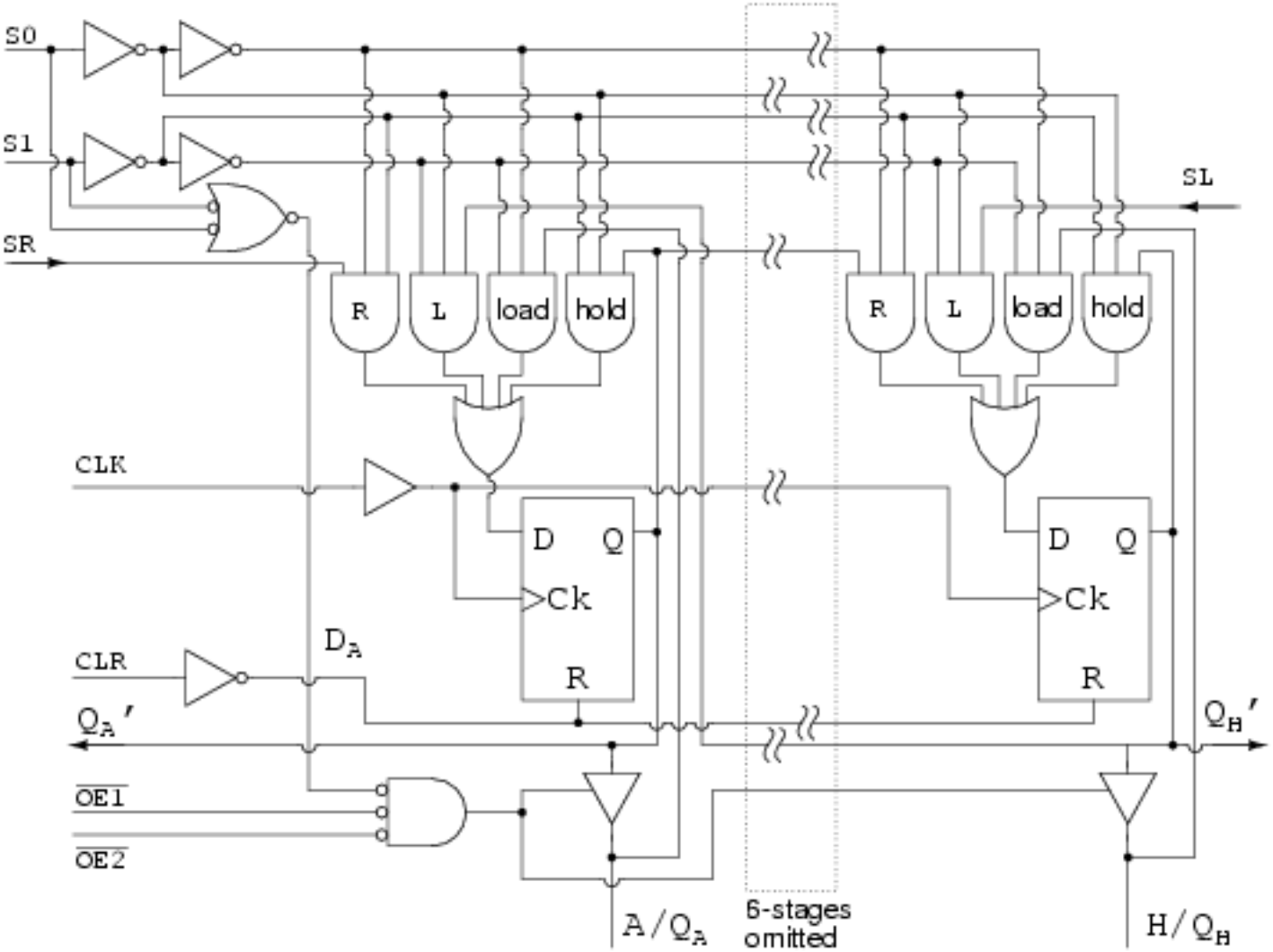
- Exemplo comercial: CI 74194

| Operating Mode | Inputs | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | $S_1$ | $S_0$ | $D_{SR}$ | $D_{SL}$ | $P_n$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| Reset | L | X | X | X | X | X | L | L | L | L |
| Hold | H | l | l | X | X | X | $q_0$ | $q_1$ | $q_2$ | $q_3$ |
| Shift Left | H | h | l | X | l | X | $q_1$ | $q_2$ | $q_3$ | L |
| | H | h | l | X | h | X | $q_1$ | $q_2$ | $q_3$ | H |
| Shift Right | H | l | h | l | X | X | L | $q_0$ | $q_1$ | $q_2$ |
| | H | l | h | h | X | X | H | $q_0$ | $q_1$ | $q_2$ |
| Parallel Load | H | h | h | X | X | $p_n$ | $p_0$ | $p_1$ | $p_2$ | $p_3$ |

H (h) = HIGH Voltage Level
L (l) = LOW Voltage Level
$p_n$ ($q_n$) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
X = Immaterial

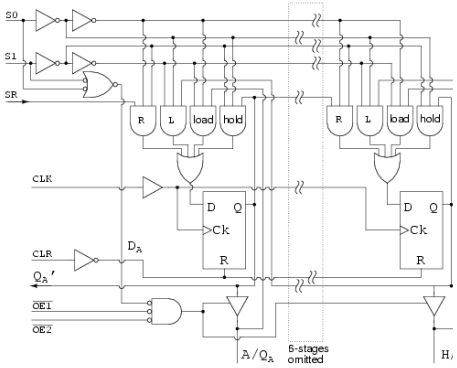


# Registrador Universal

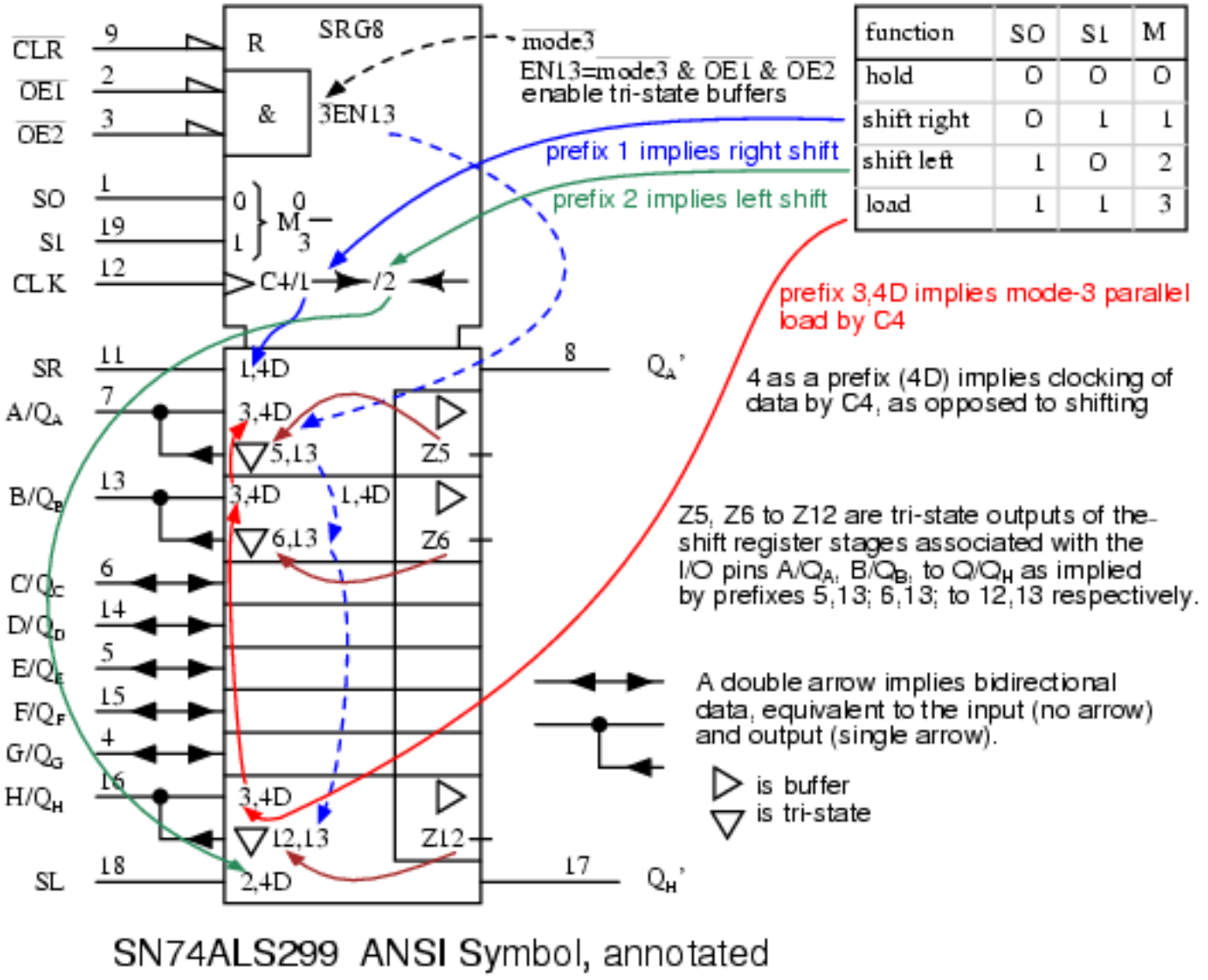



74ALS299 universal shift/ storage register with tri-state outputs

# Registrador Universal



74ALS299 universal shift/ storage register with tri-state outputs




| function | SO | S1 | M |
|---|---|---|---|
| hold | 0 | 0 | 0 |
| shift right | 0 | 1 | 1 |
| shift left | 1 | 0 | 2 |
| load | 1 | 1 | 3 |

SN74ALS299 ANSI Symbol, annotated

# Outros registradores "universais"

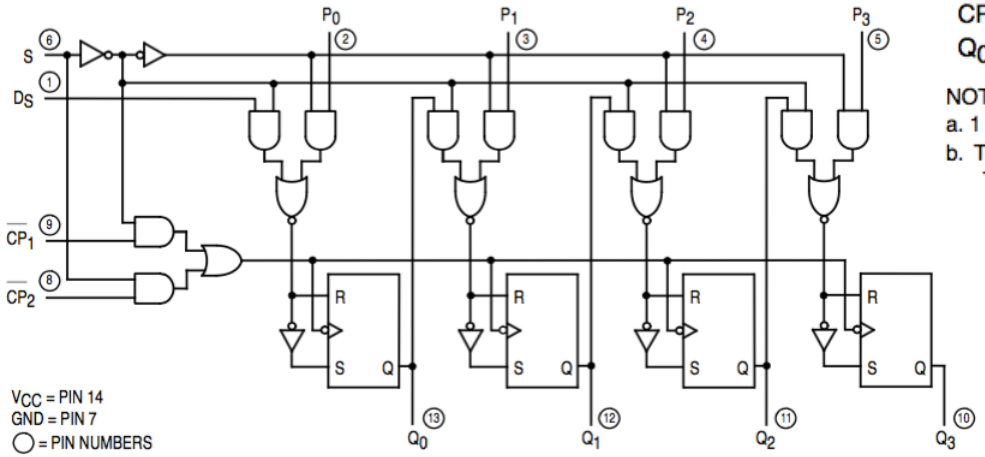
- 74LS95B:

## 4-BIT SHIFT REGISTER

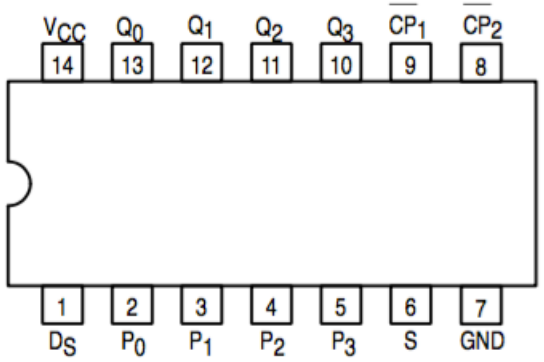
The SN54/74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The LS95B is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Synchronous, Expandable Shift Right
- Synchronous Shift Left Capability
- Synchronous Parallel Load
- Separate Shift and Load Clock Inputs
- Input Clamp Diodes Limit High Speed Termination Effects




**CONNECTION DIAGRAM DIP** (TOP VIEW)




NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

$V_{CC}$ = PIN 14
GND = PIN 7

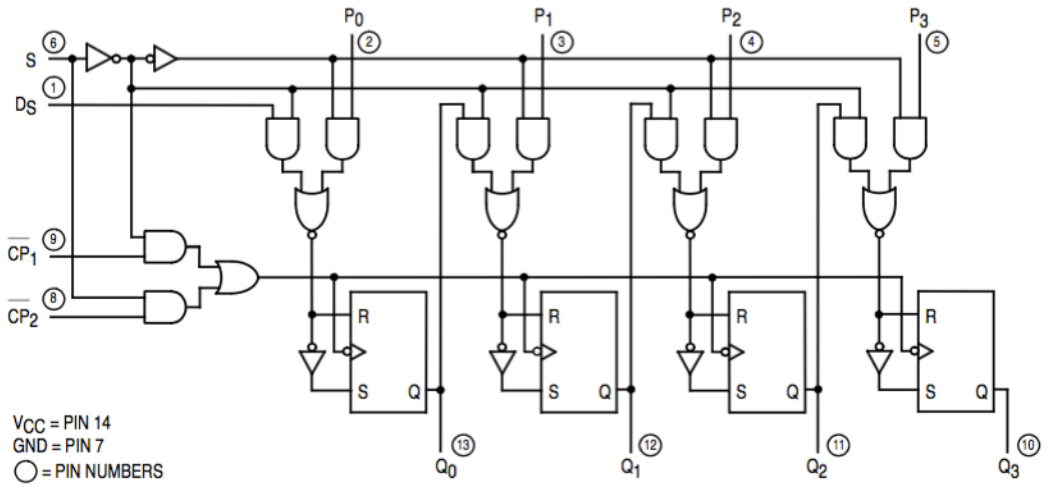
**PIN NAMES**

| | | **LOADING** (Note a) HIGH | LOW |
|---|---|---|---|
| S | Mode Control Input | 0.5 U.L. | 0.25 U.L. |
| $D_S$ | Serial Data Input | 0.5 U.L. | 0.25 U.L. |
| $P_0$–$P_3$ | Parallel Data Inputs | 0.5 U.L. | 0.25 U.L. |
| $\overline{CP}_1$ | Serial Clock (Active LOW Going Edge) Input | 0.5 U.L. | 0.25 U.L. |
| $CP_2$ | Parallel Clock (Active LOW Going Edge) Input | 0.5 U.L. | 0.25 U.L. |
| $Q_0$–$Q_3$ | Parallel Outputs (Note b) | 10 U.L. | 5 (2.5) U.L. |

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

# Outros registradores "universais"

- 74LS95B:




**PIN NAMES**

| | |
|---|---|
| S | Mode Control Input |
| $D_S$ | Serial Data Input |
| $P_0$–$P_3$ | Parallel Data Inputs |
| $\overline{CP}_1$ | Serial Clock (Active LOW Going Edge) Input |
| $CP_2$ | Parallel Clock (Active LOW Going Edge) Input |
| $Q_0$–$Q_3$ | Parallel Outputs (Note b) |

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

**MODE SELECT — TRUTH TABLE**

| OPERATING MODE | INPUTS | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|
| | S | $CP_1$ | $CP_2$ | $D_S$ | $P_n$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| Shift | L | ↓ | X | l | X | L | $q_0$ | $q_1$ | $q_2$ |
| | L | ↓ | X | h | X | H | $q_0$ | $q_1$ | $q_2$ |
| Parallel Load | H | X | ↓ | X | $P_n$ | $P_0$ | $P_1$ | $P_2$ | $P_3$ |
| Mode Change | ↓ | L | L | X | X | No Change | | | |
| | ↑ | L | L | X | X | No Change | | | |
| | ↓ | H | L | X | X | No Change | | | |
| | ↑ | H | L | X | X | Undetermined | | | |
| | ↓ | L | H | X | X | Undetermined | | | |
| | ↑ | L | H | X | X | No Change | | | |
| | ↓ | H | H | X | X | Undetermined | | | |
| | ↑ | H | H | X | X | No Change | | | |

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.
$P_n$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.