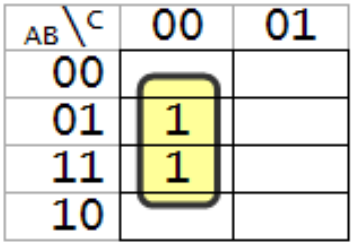
Aplicações de Mapas de Karnaugh

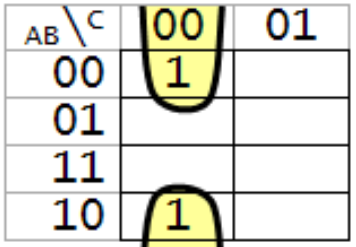
Circuitos Digitais I
Prof. Fernando Passold

Resumo de Mapas de Karnaugh:

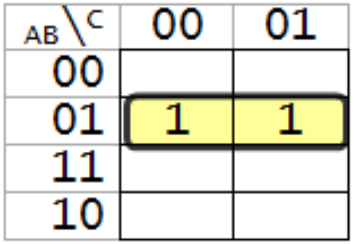
- Agrupamentos de **2** células:



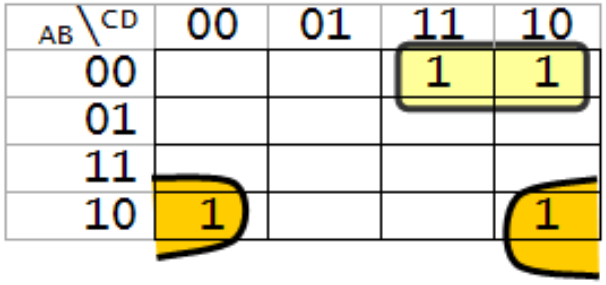
$x = B\overline{C}$



$x = \overline{B}\overline{C}$



$x = \overline{A}B$



$x = \overline{A}\overline{B}C + A\overline{B}\overline{D}$

Resumo de Mapas de Karnaugh:

- Agrupamentos de **4** células:

AB \ C	00	01
00		1
01		1
11		1
10		1

$x = C$

AB \ CD	00	01	11	10
00				
01				
11	1	1	1	1
10				

$x = AB$

AB \ CD	00	01	11	10
00				
01		1	1	
11		1	1	
10				

$x = BD$

AB \ CD	00	01	11	10
00				
01				
11	1			1
10	1			1

$x = A\overline{D}$

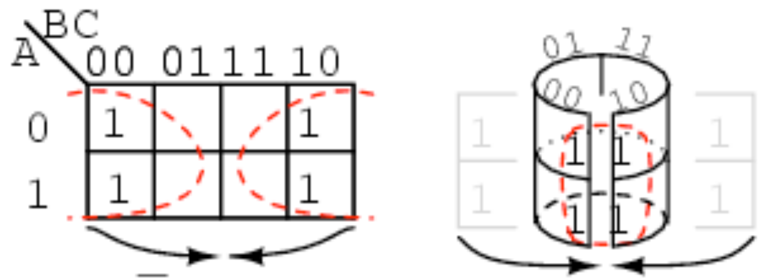
AB \ CD	00	01	11	10
00	1			1
01				
11				
10	1			1

$x = \overline{B}\overline{D}$

Resumo de Mapas de Karnaugh:

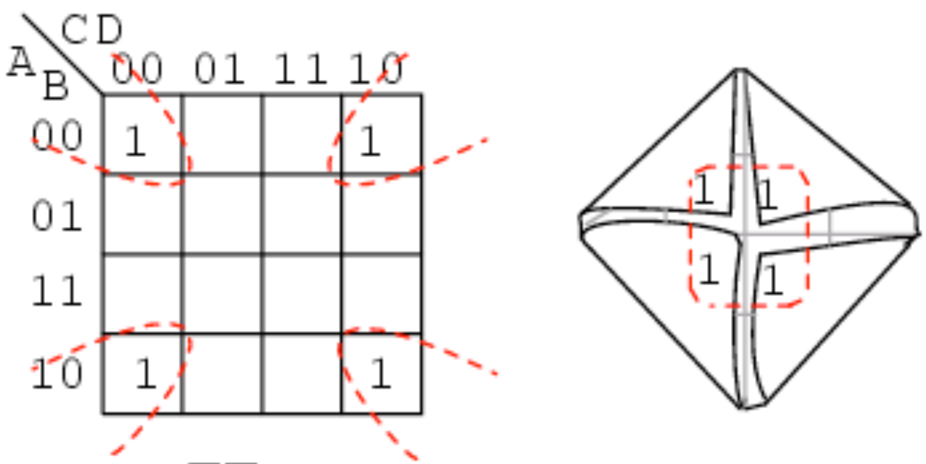
- Agrupamentos de **4** células:

$$Out = \overline{A}\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C} + A\,B\,\overline{C}$$



$$Out = \overline{C}$$

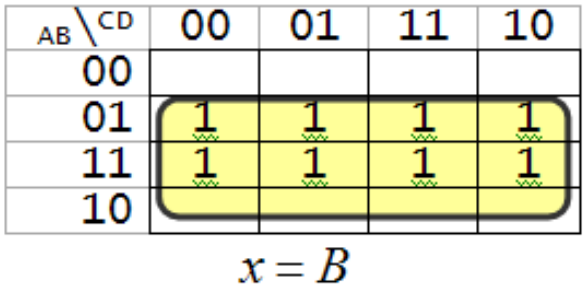
$$Out = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,C\,\overline{D} + A\,\overline{B}\,\overline{C}\,\overline{D} + A\,\overline{B}\,C\,\overline{D}$$

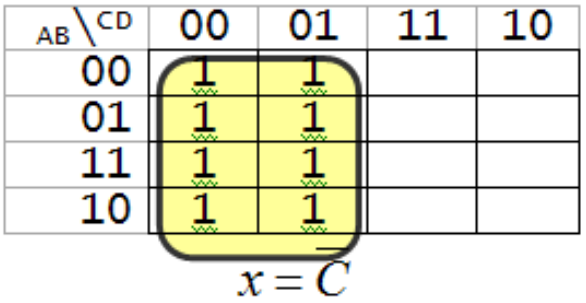


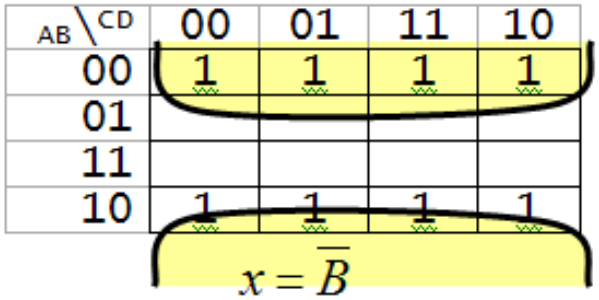
$$Out = \overline{B}\,\overline{D}$$

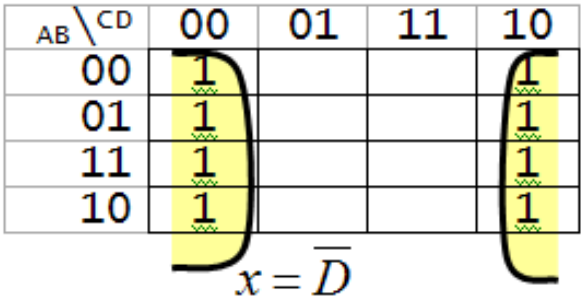
Resumo de Mapas de Karnaugh:

- Agrupamentos de **8** células:



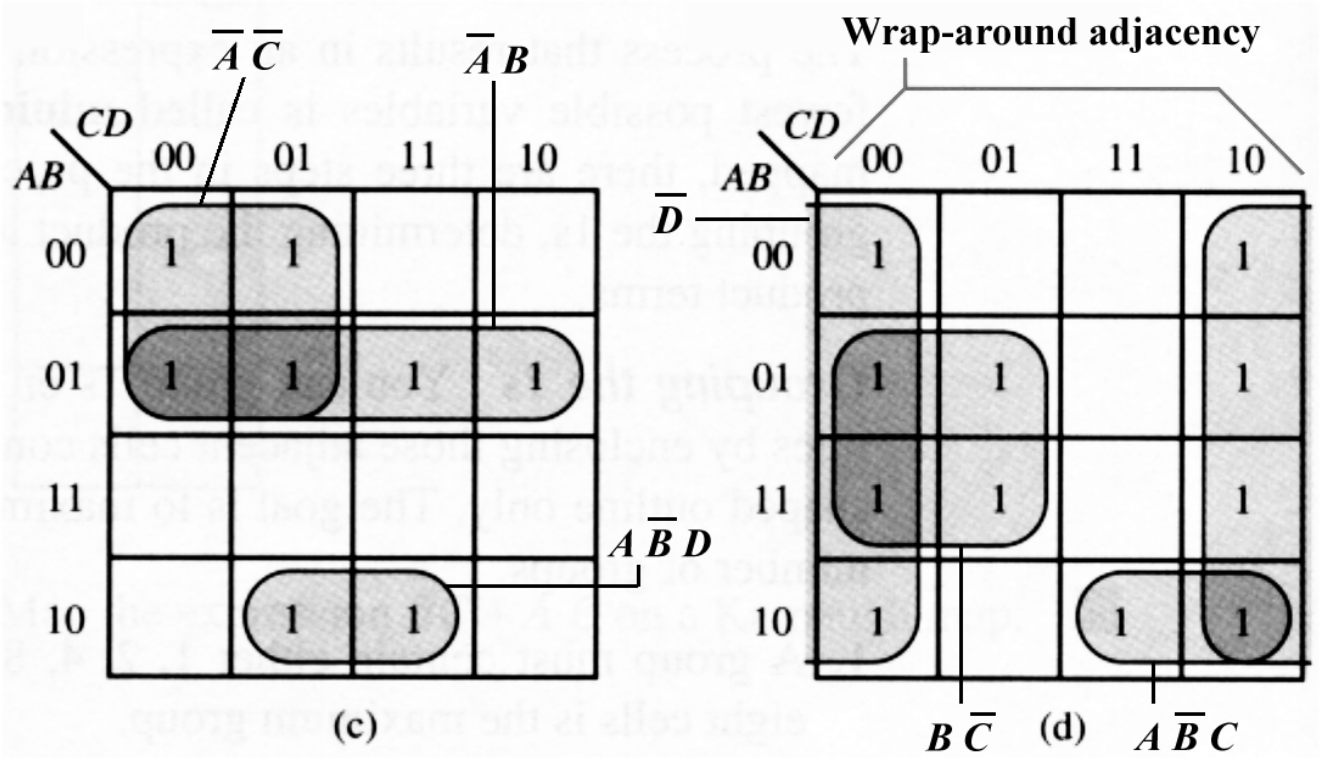






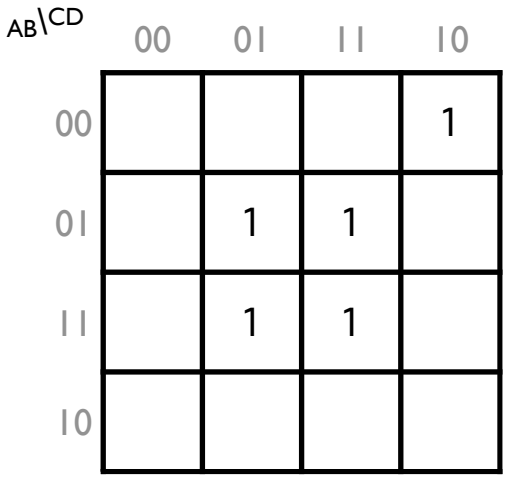
Mapas de Karnaugh:

- Exemplos de Simplificações possíveis:



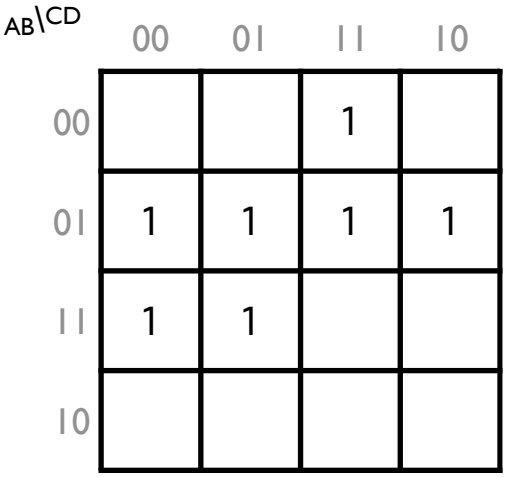
Mapas de Karnaugh:

- Exemplos de Simplificações possíveis:



$$X = \underbrace{\bar{A}\bar{B}C\bar{D}}_{\text{loop 4}} + \underbrace{ACD}_{\text{loop 11, 15}} + \underbrace{BD}_{\text{loop 6, 7, 10, 11}}$$

(a)

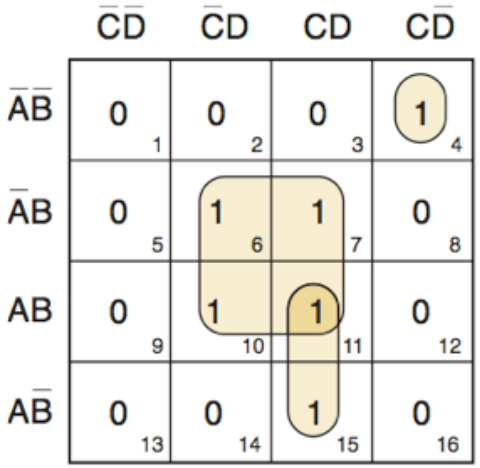


$$X = \underbrace{\bar{A}B}_{\text{loop 5, 6, 7, 8}} + \underbrace{B\bar{C}}_{\text{loop 5, 6, 9, 10}} + \underbrace{\bar{A}CD}_{\text{loop 3,7}}$$

(b)

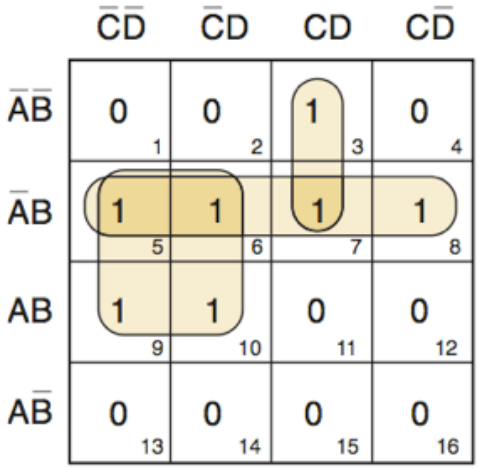
Mapas de Karnaugh:

- Exemplos de Simplificações possíveis:



$$X = \underbrace{\bar{A}\bar{B}C\bar{D}}_{\text{loop 4}} + \underbrace{ACD}_{\text{loop 11, 15}} + \underbrace{BD}_{\text{loop 6, 7, 10, 11}}$$

(a)



$$X = \underbrace{\bar{A}B}_{\text{loop 5, 6, 7, 8}} + \underbrace{B\bar{C}}_{\text{loop 5, 6, 9, 10}} + \underbrace{\bar{A}CD}_{\text{loop 3,7}}$$

(b)

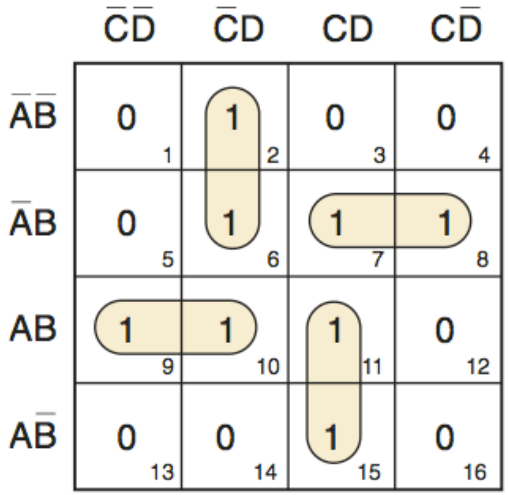
Mapas de Karnaugh:

- Exemplos de Simplificações possíveis:

AB\CD	00	01	11	10
00		1		
01		1	1	1
11	1	1	1	
10			1	

Mapas de Karnaugh:

- Exemplos de Simplificações possíveis:



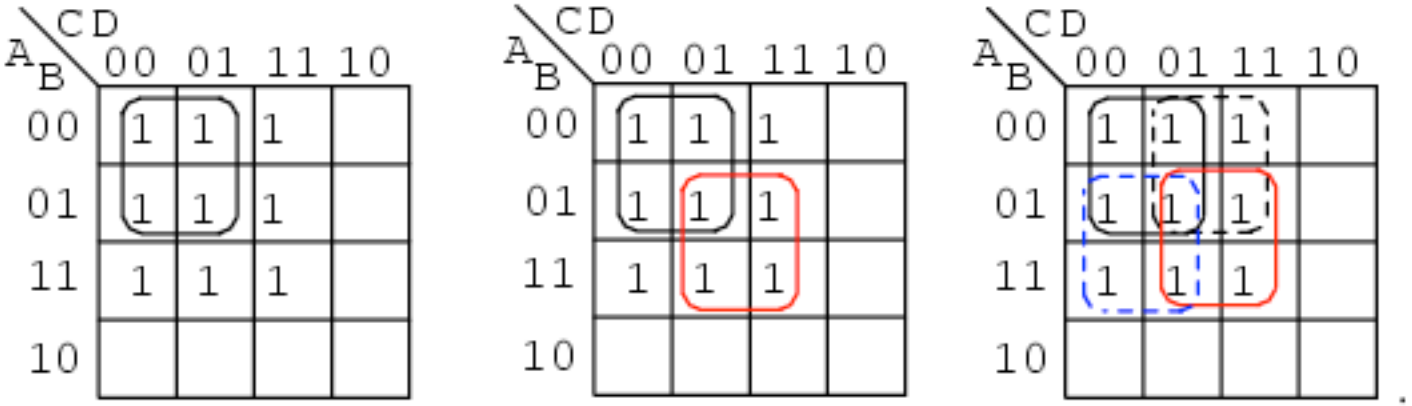
(c)

$$X = \underbrace{AB\bar{C}}_{9,\,10} + \underbrace{\bar{A}\bar{C}D}_{2,\,6} + \underbrace{\bar{A}BC}_{7,\,8} + \underbrace{ACD}_{11,\,15}$$

Mapas de Karnaugh:

- Exemplos de Simplificações possíveis:

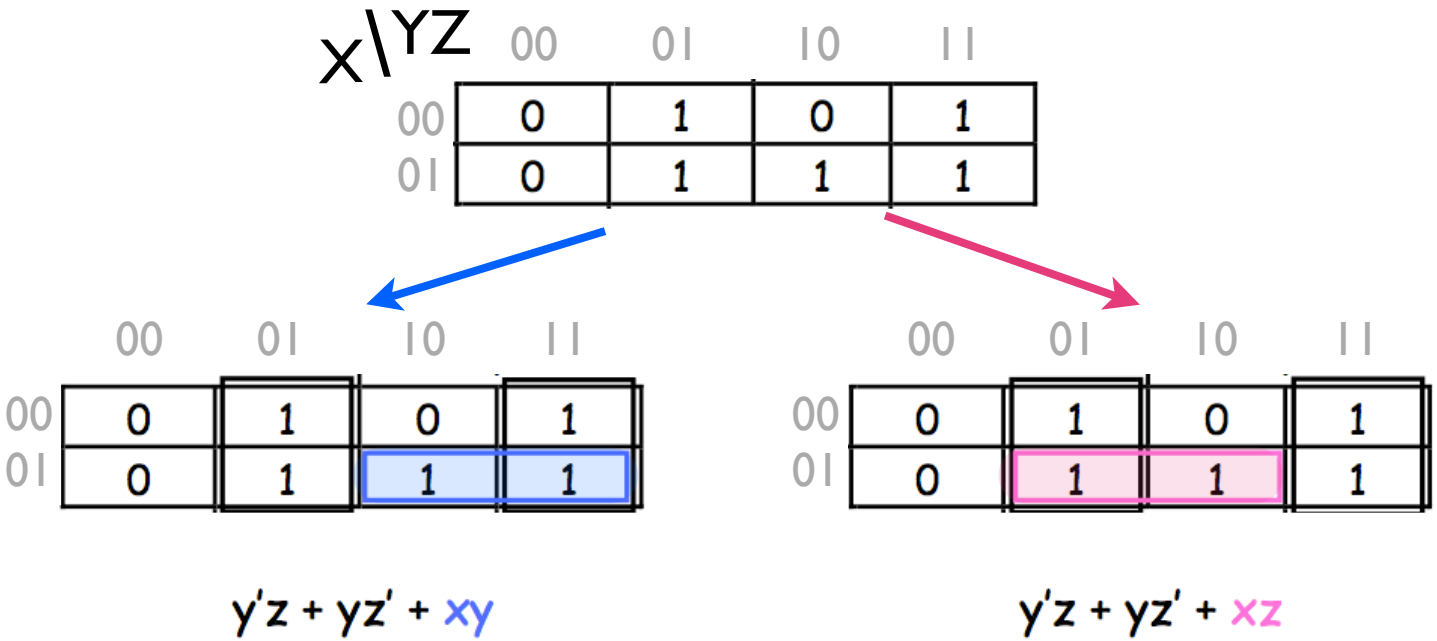
$$Out = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}C\,\overline{D} + \overline{A}\,\overline{B}CD + \overline{A}B\,\overline{C}\,\overline{D} + \overline{A}B\,\overline{C}D + \overline{A}BC\,\overline{D} + \overline{A}BCD + A\,\overline{B}\,\overline{C}\,\overline{D} + A\,\overline{B}\,\overline{C}D + A\,\overline{B}C\,\overline{D} + A\,\overline{B}CD + AB\,\overline{C}\,\overline{D} + AB\,\overline{C}D + ABC\,\overline{D} + ABCD$$



$$Out = \overline{A}\,\overline{C} + \overline{A}D + B\,\overline{C} + BD$$

Mapas de Karnaugh:

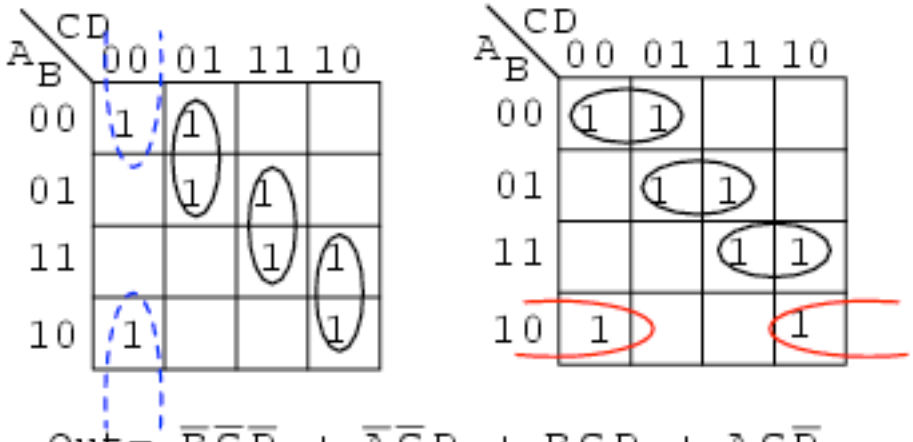
- Exemplo de 2 soluções igualmente possíveis:



Mapas de Karnaugh:

- Exemplo de 2 soluções igualmente possíveis:

$$Out = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}D + \overline{A}B\overline{C}D + \overline{A}BCD + ABCD + ABC\overline{D} + A\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}C\overline{D}$$



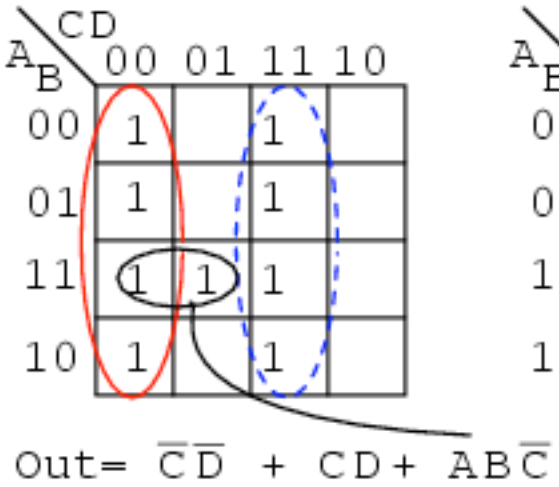
$$Out = \overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{C}D + BCD + AC\overline{D}$$

$$Out = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}BD + ABC + A\overline{B}\,\overline{D}$$

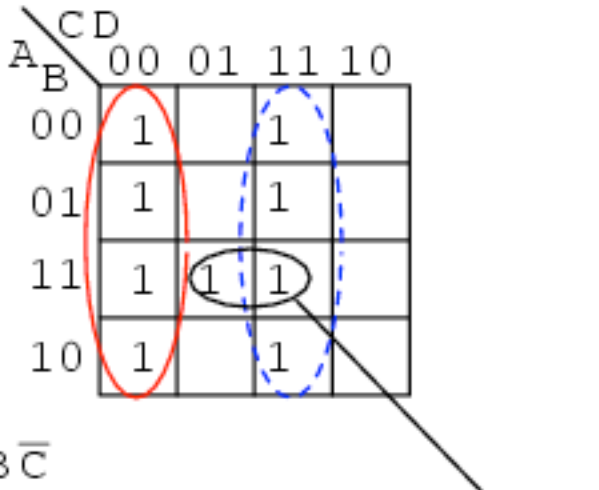
Mapas de Karnaugh:

- Exemplo de 2 soluções igualmente possíveis:

$$Out = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + \bar{A}BCD + AB\bar{C}\bar{D} + AB\bar{C}D + ABCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}CD$$



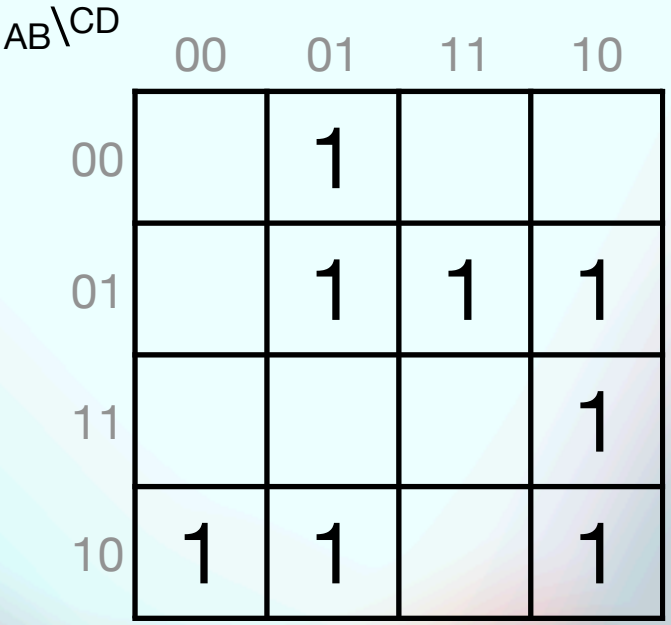
$$Out = \bar{C}\bar{D} + CD + A\bar{B}\bar{C}$$



$$Out = \bar{C}\bar{D} + CD + ABD$$

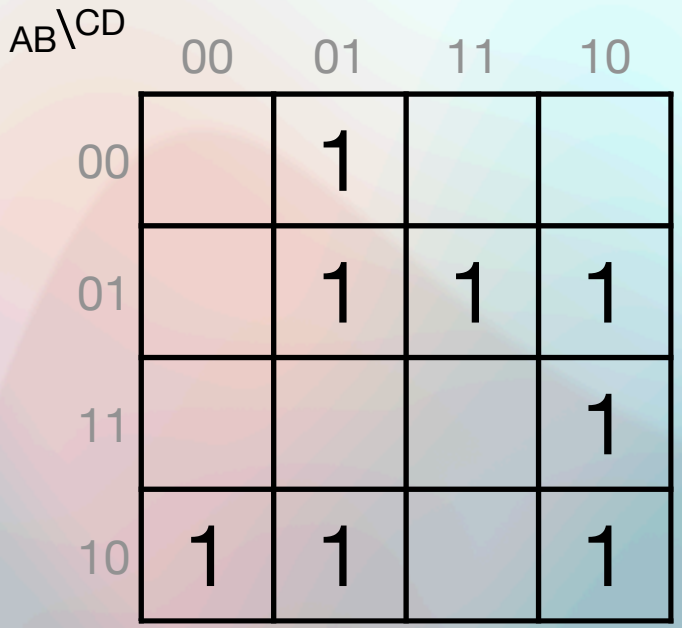
Mapas de Karnaugh:

- Exemplo de 2 soluções igualmente muito boas:



$X = \bar{A}\bar{C}D + \bar{A}BC + A\bar{B}\bar{C} + AC\bar{D}$

(a)

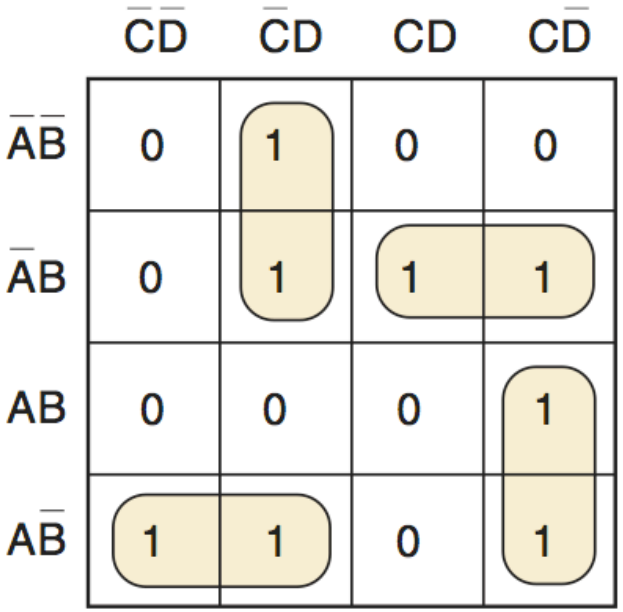


$X = \bar{A}BD + B\bar{C}D + \bar{B}\bar{C}D + A\bar{B}\bar{D}$

(b)

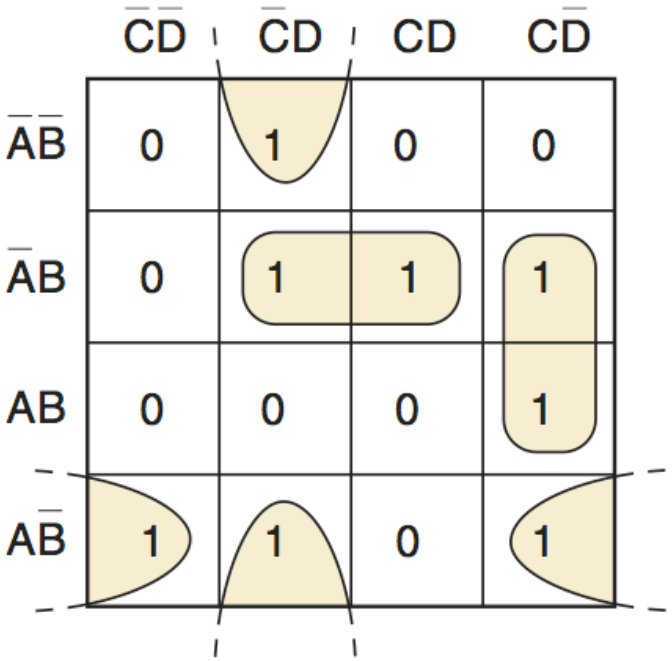
Mapas de Karnaugh:

- Exemplo de 2 soluções igualmente muito boas:



$$X = \bar{A}\bar{C}D + \bar{A}BC + A\bar{B}\bar{C} + AC\bar{D}$$

(a)



$$X = \bar{A}BD + BC\bar{D} + \bar{B}\bar{C}D + A\bar{B}\bar{D}$$

(b)

Circuito (a):
1 x OR(4)+4xAND(3)+4xNOT

Circuito (b):
1 x OR(4)+4xAND(3)+4xNOT

Problema

- Projete o circuito lógico que possui 4 entradas (A, B, C e D) e que seja capaz de detectar as situações nas quais apenas 2 variáveis de entrada estão ativadas. Obs: D=MSB, A=LSB.

Ref	DCBA	Z
0	0000	
1	0001	
2	0010	
3	0011	
4	0100	
5	0101	
6	0110	
7	0111	
8	1000	
9	1001	
10	1010	
11	1011	
12	1100	
13	1101	
14	1110	
15	1111	

$$Z = \bar{D}\bar{C}BA + (B \oplus A)(D \oplus C) + DC\bar{B}\bar{A}$$

Problema

- Projete o circuito lógico que possui 4 entradas (A, B, C e D) e que seja capaz de detectar as situações nas quais apenas 2 variáveis de entrada estão ativadas. Obs: D=MSB, A=LSB.

Ref	DCBA	Z	
0	0000		
1	0001		
2	0010		
3	0011	1	$= \bar{D}\bar{C}BA$
4	0100		
5	0101	1	$= \bar{D}C\bar{B}A$
6	0110	1	$= \bar{D}CB\bar{A}$
7	0111		
8	1000		
9	1001	1	$= D\bar{C}\bar{B}A$
10	1010	1	$= D\bar{C}B\bar{A}$
11	1011		
12	1100	1	$= DC\bar{B}\bar{A}$
13	1101		
14	1110		
15	1111		

Z: DC\BA

	00	01	11	10
00	0	1	1 3	2
01	4	1 5	7	1 6
11	1 12	13	15	14
10	8	1 9	11	1 10

$$Z = \underbrace{\bar{D}\bar{C}BA}_{m_3} + \underbrace{\bar{D}C\bar{B}A}_{m_5} + \underbrace{\bar{D}CB\bar{A}}_{m_6} + \underbrace{D\bar{C}\bar{B}A}_{m_9} + \underbrace{D\bar{C}B\bar{A}}_{m_{10}} + \underbrace{DC\bar{B}\bar{A}}_{m_{12}}$$

$$Z = \bar{D}\bar{C}BA + \bar{D}C(\bar{B}A + B\bar{A}) + D\bar{C}(\bar{B}A + B\bar{A}) + DC\bar{B}\bar{A}$$

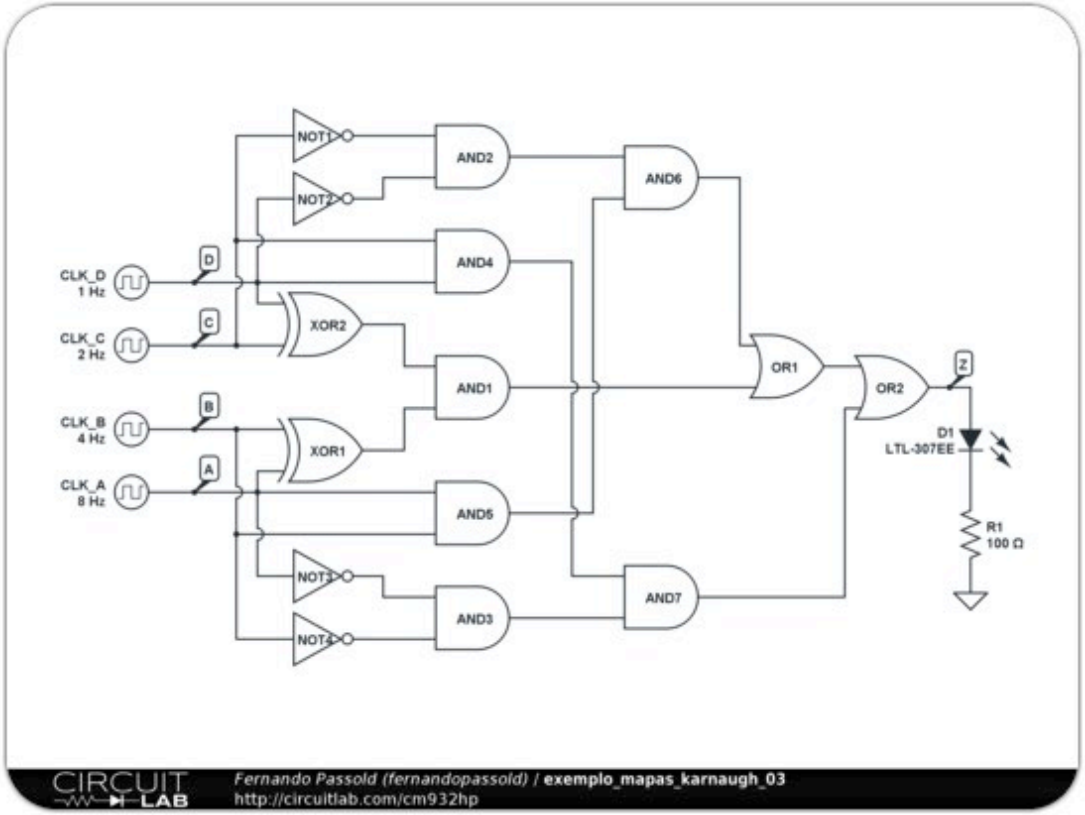
$$Z = \bar{D}\bar{C}BA + \bar{D}C(B \oplus A) + D\bar{C}(B \oplus A) + DC\bar{B}\bar{A}$$

$$Z = \bar{D}\bar{C}BA + (B \oplus A)(\bar{D}C + D\bar{C}) + DC\bar{B}\bar{A}$$

$$Z = \bar{D}\bar{C}BA + (B \oplus A)(D \oplus C) + DC\bar{B}\bar{A}$$

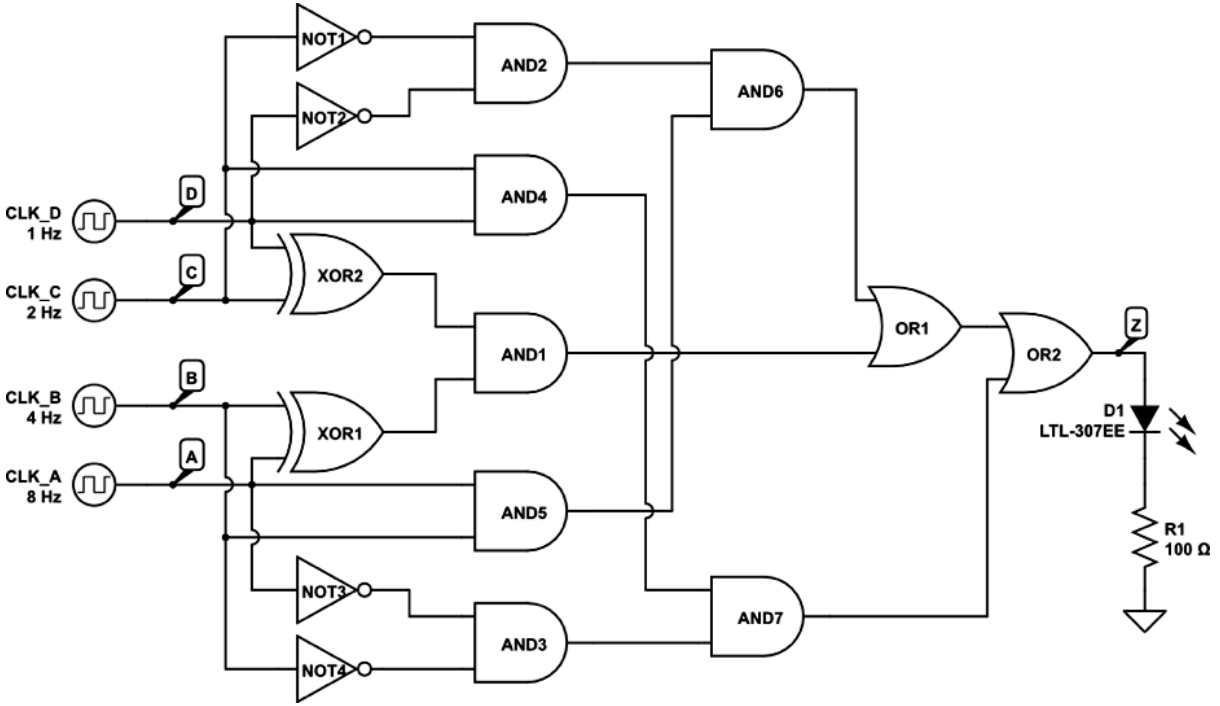
Problema

- Projete o circuito lógico que possui 4 entradas (A, B, C e D) e que seja capaz de detectar as situações nas quais apenas 2 variáveis de entrada estão ativadas. Obs: D=MSB. A=LSB.



- Solução --> Circuito: disponível em: https://www.circuitlab.com/circuit/m932hp/exemplo_mapas_karnaugh_03/ (em 13/set/2013)

- Uso do CircuitLab (web-based electronics design tool): www.circuitlab.com



CIRCUIT LAB File Edit Run

- DC
- DC Sweep
- Time Domain

Start Time: 0 s

Stop Time: 1.2 s

Time Step: 1 s

Skip Initial: No

Sweep Parameter:

Outputs:

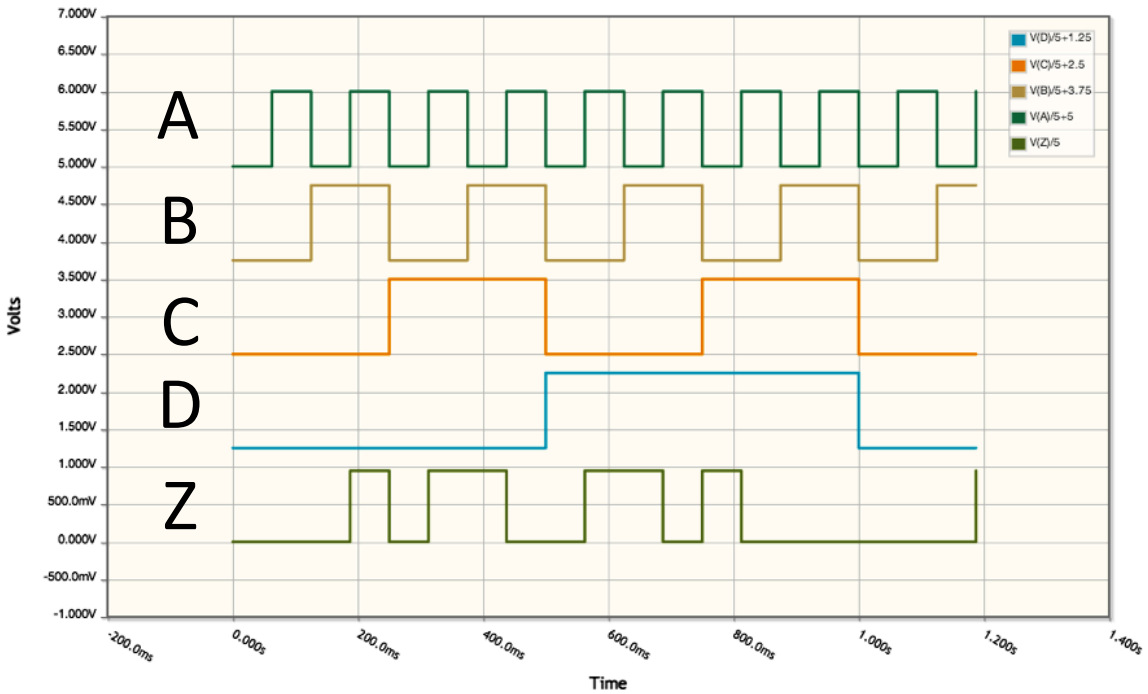
- V(D)/5+1.25
- V(C)/5+2.5
- V(B)/5+3.75
- V(A)/5+5
- V(Z)/5

+ Add Expression

Advanced Graphing...

Run Time-Domain Simulation

- Frequency Domain



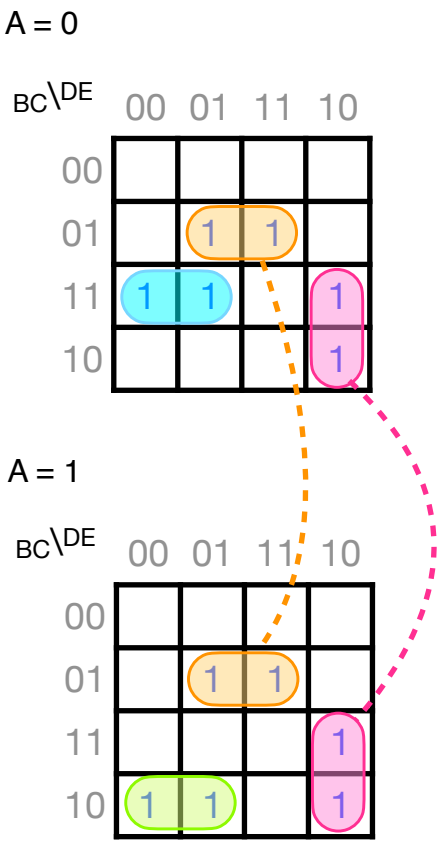
Mapas K para 5 variáveis

- 2 opções:
  Repare na seq. dos códigos

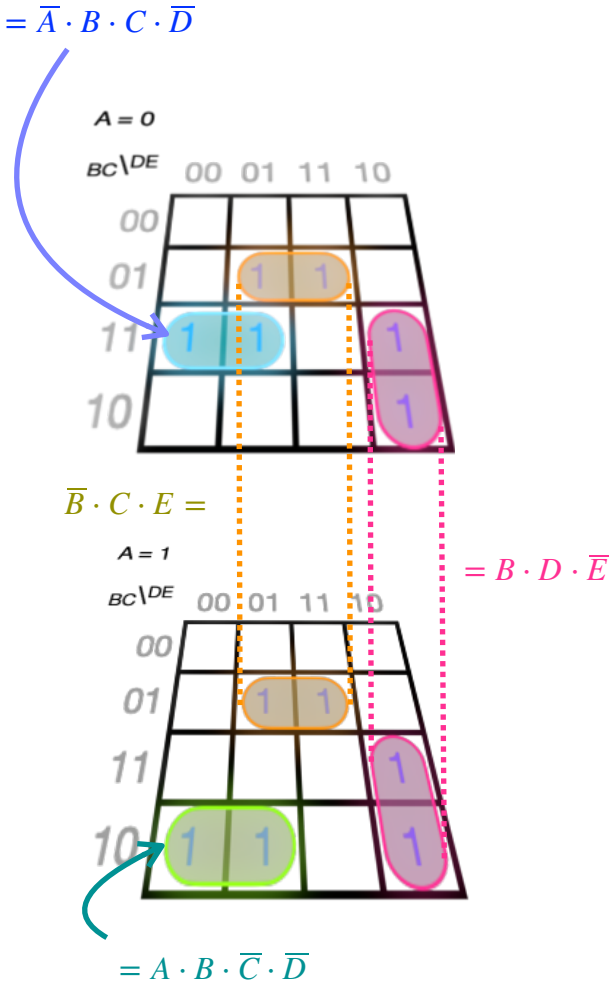
Repare:
A=bit mais significativo!

Tabela Verdade

Ref	ABCDE	Y
0	00000	
1	1	
:	:	
15	01111	
16	10000	
17	10001	
:	:	
30	11110	
31	11111	



Método "camadas" (overlay)



Mapas K para 5 variáveis

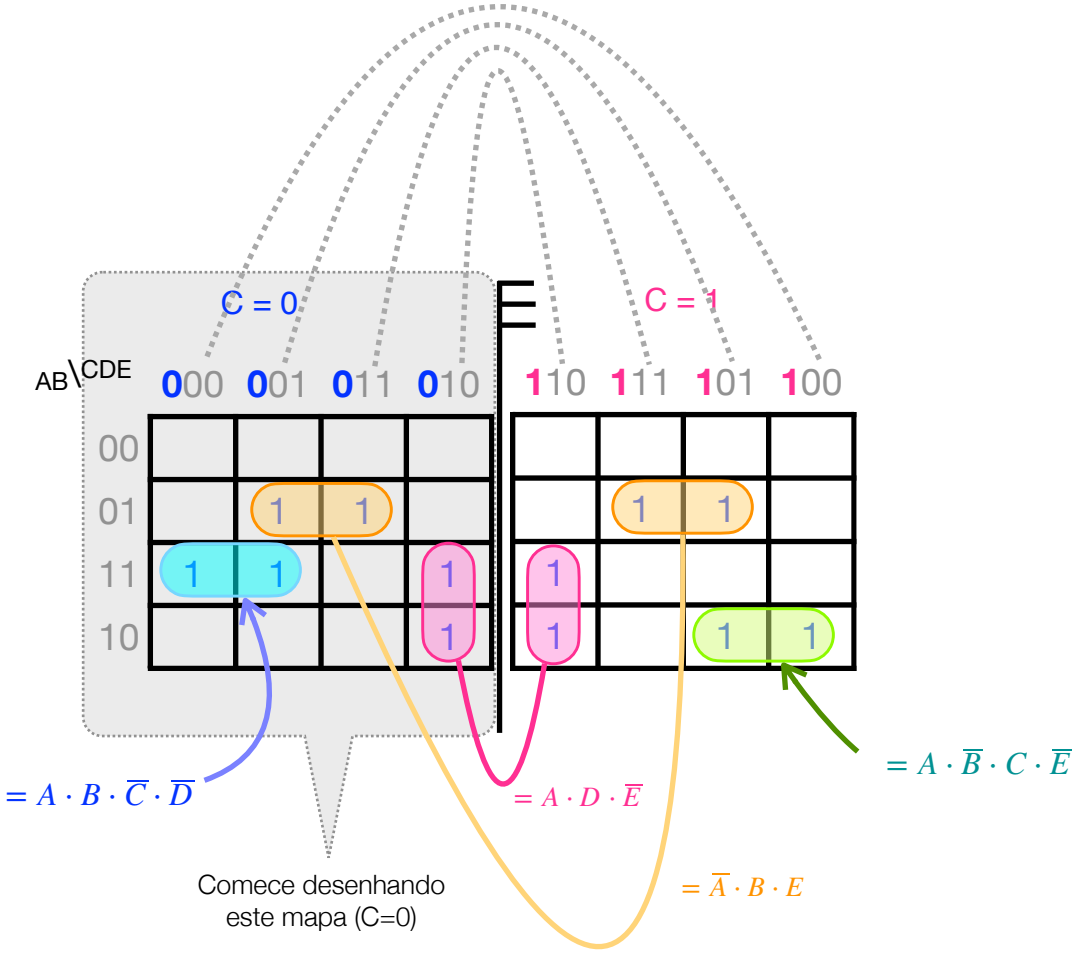
- 2 opções:
  Repare na seq. dos códigos

Repare:
A=bit mais significativo!

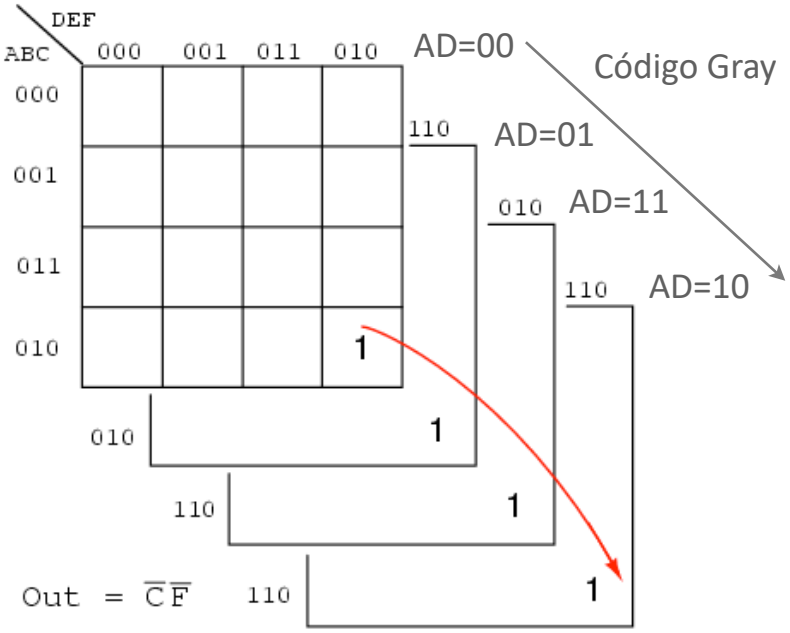
Tabela Verdade

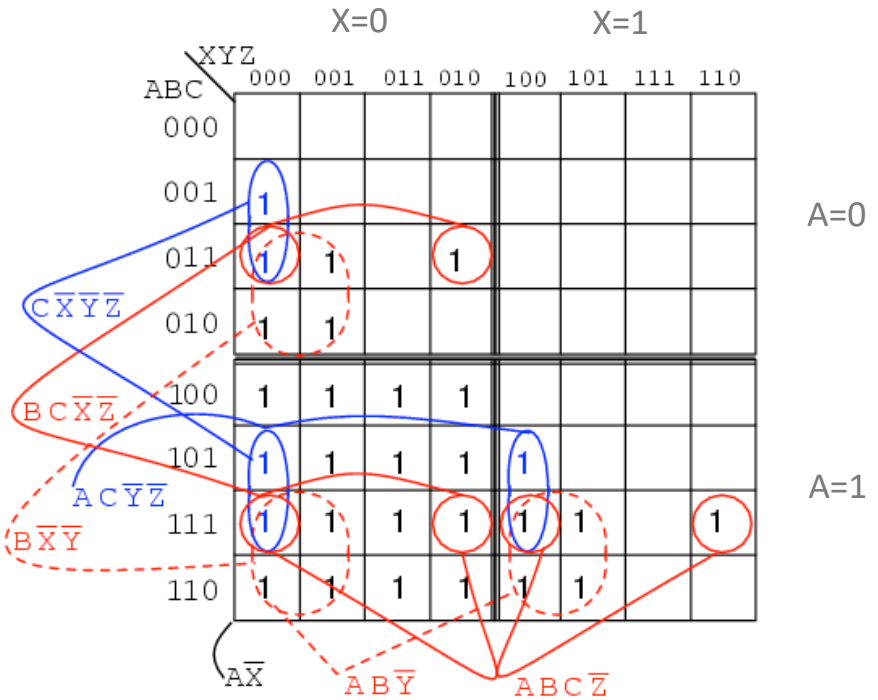
Ref	ABCDE	Y
0	00000	
1	1	
:	:	
15	01111	
16	10000	
17	10001	
:	:	
30	11110	
31	11111	

Método "espelho" (mirror)



Mapas K para 6 variáveis

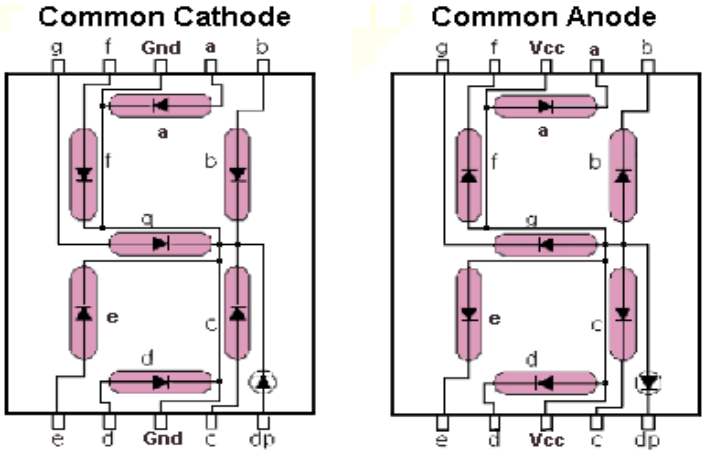


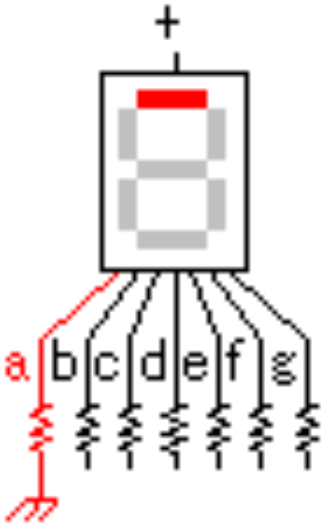


Out = $A\overline{X} + AB\overline{Y} + B\overline{X}\,\overline{Y} + ABC\overline{Z} + AC\overline{Y}\,\overline{Z} + BC\overline{X}\,\overline{Z} + C\overline{X}\,\overline{Y}\,\overline{Z}$

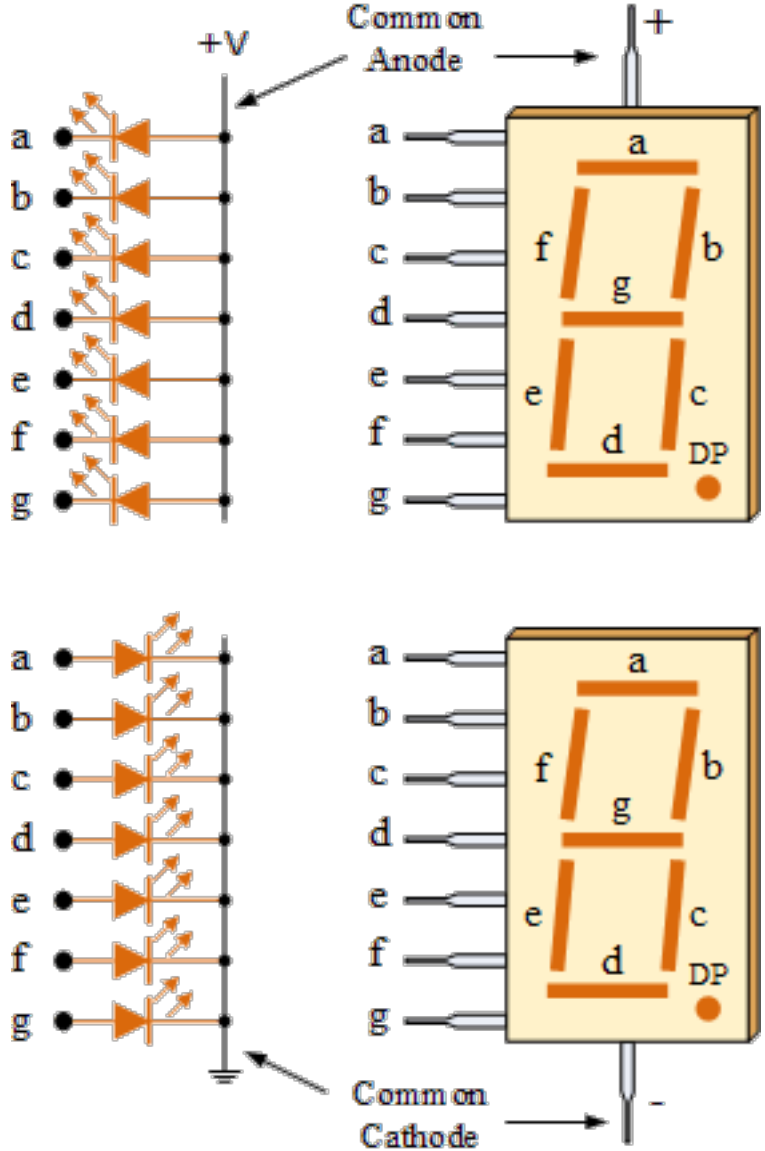
6- variable Karnaugh map (overlay)

DEC Display 7 Segmentos

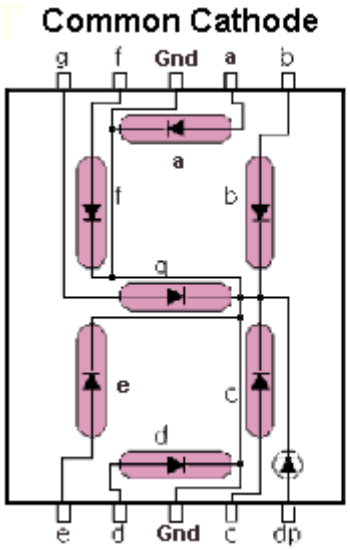


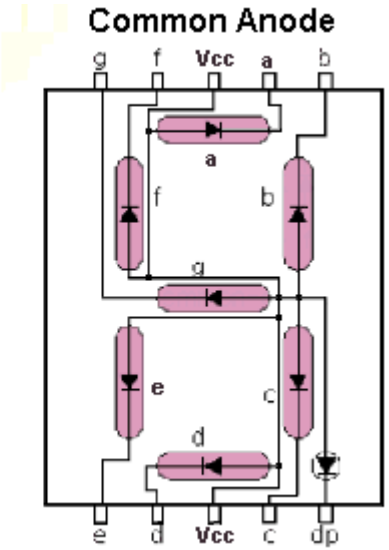


Ânodo comum



Display 7 Segmentos / BCD





DECIMAL	DCBA
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

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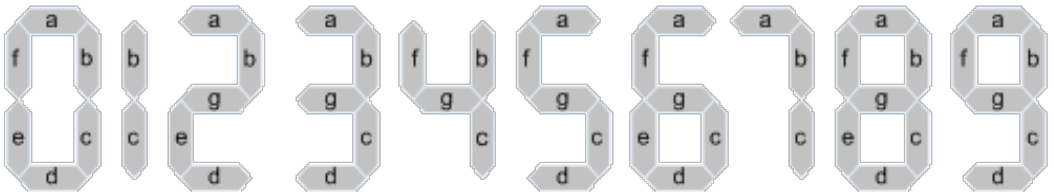
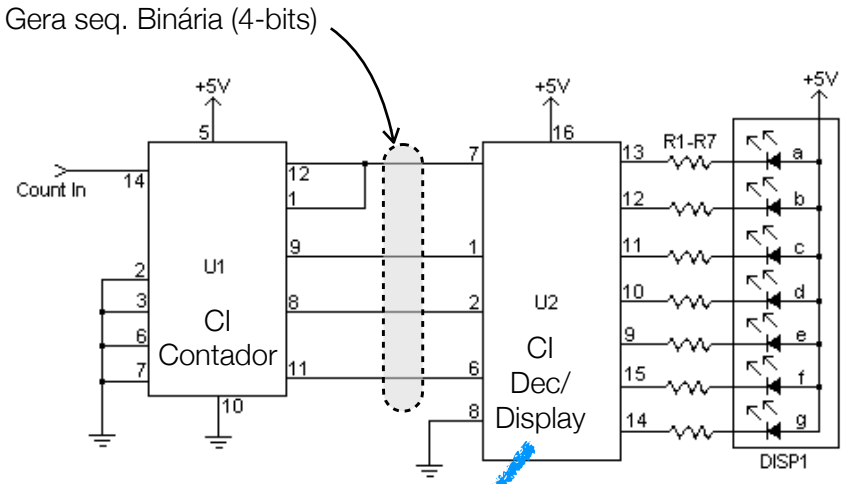
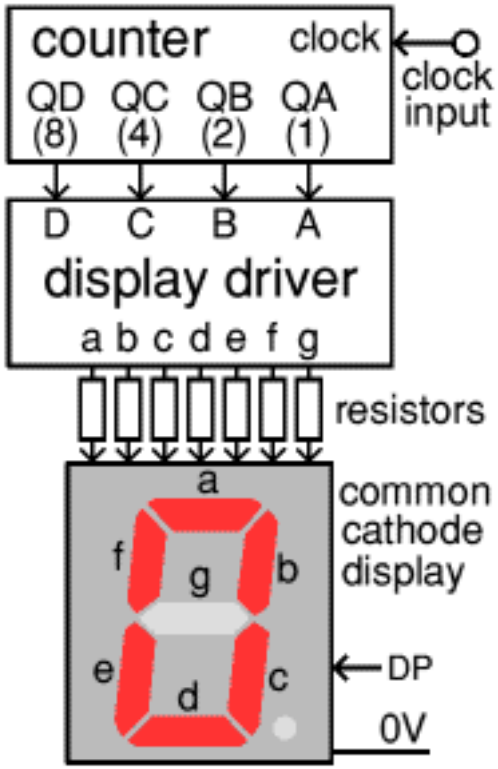
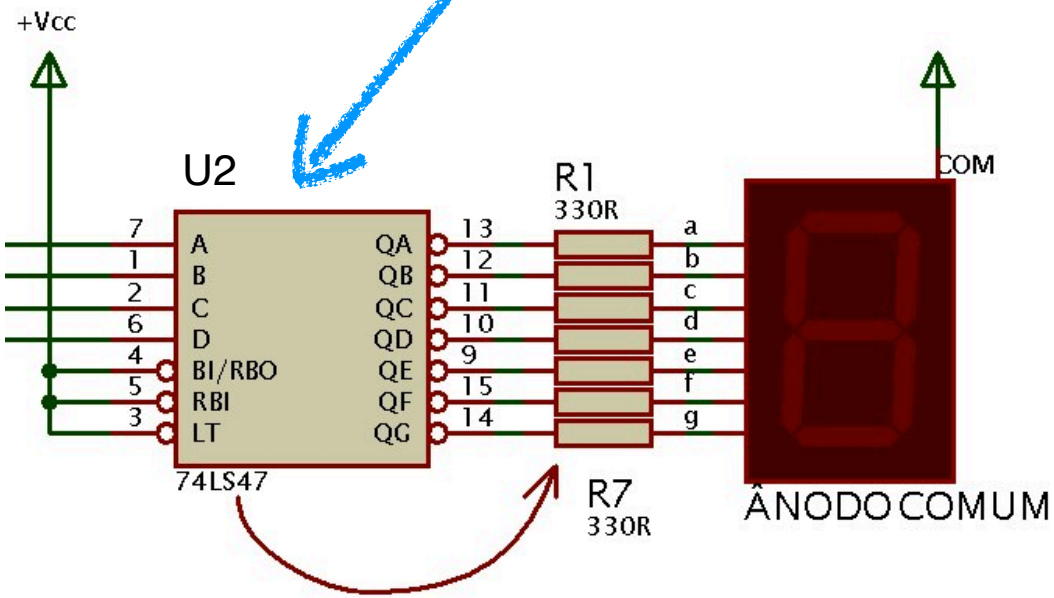
Digit Shown	Illuminated Segment (1 = illumination)						
	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	0	1	0	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1



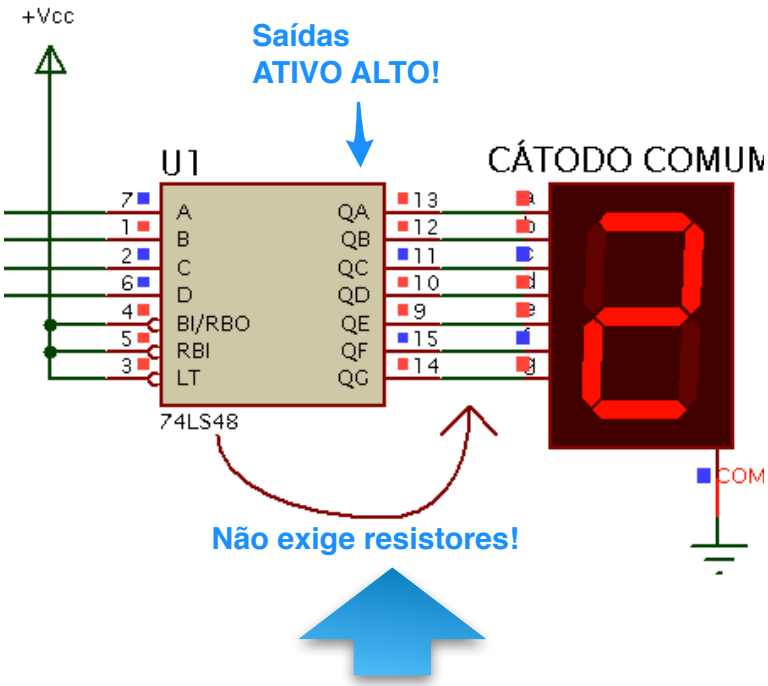
DEC Display 7







DEC Display



Obs.: mas apenas o CI 74LS48!

MOTOROLA

BCD TO 7-SEGMENT DECODER

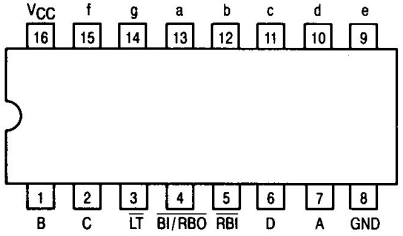
The SN54/74LS48 is a BCD to 7-Segment Decoder consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking input for the LS48.

The circuit accepts 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive other components. The relative positive logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables.

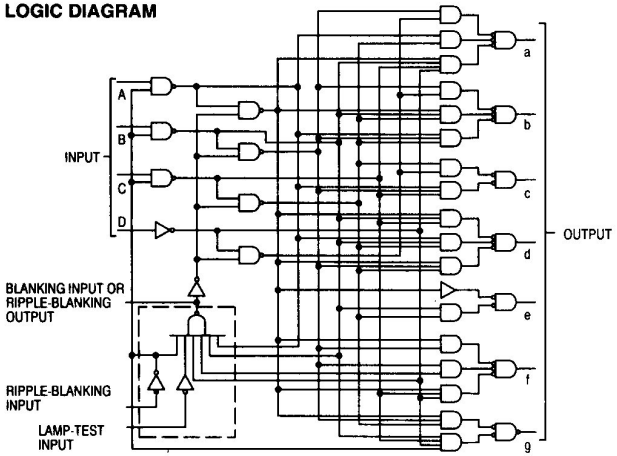
The LS48 circuit incorporates automatic leading and/or trailing edge zero-blanking control (RBI and RBO). Lamp Test (LT) may be activated any time when the BI/RBO node is HIGH. Both devices contain an overriding blanking input (BI) which can be used to control the lamp intensity by varying the frequency and duty cycle of the BI input signal or to inhibit the outputs.

- Lamp Intensity Modulation Capability (BI/RBO)
- Internal Pull-Ups Eliminate Need for External Resistors
- Input Clamp Diodes Eliminate High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



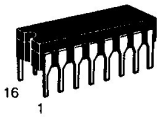
LOGIC DIAGRAM



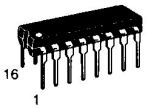
SN54/74LS48

BCD TO 7-SEGMENT DECODER

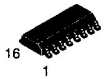
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

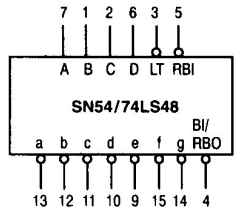


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

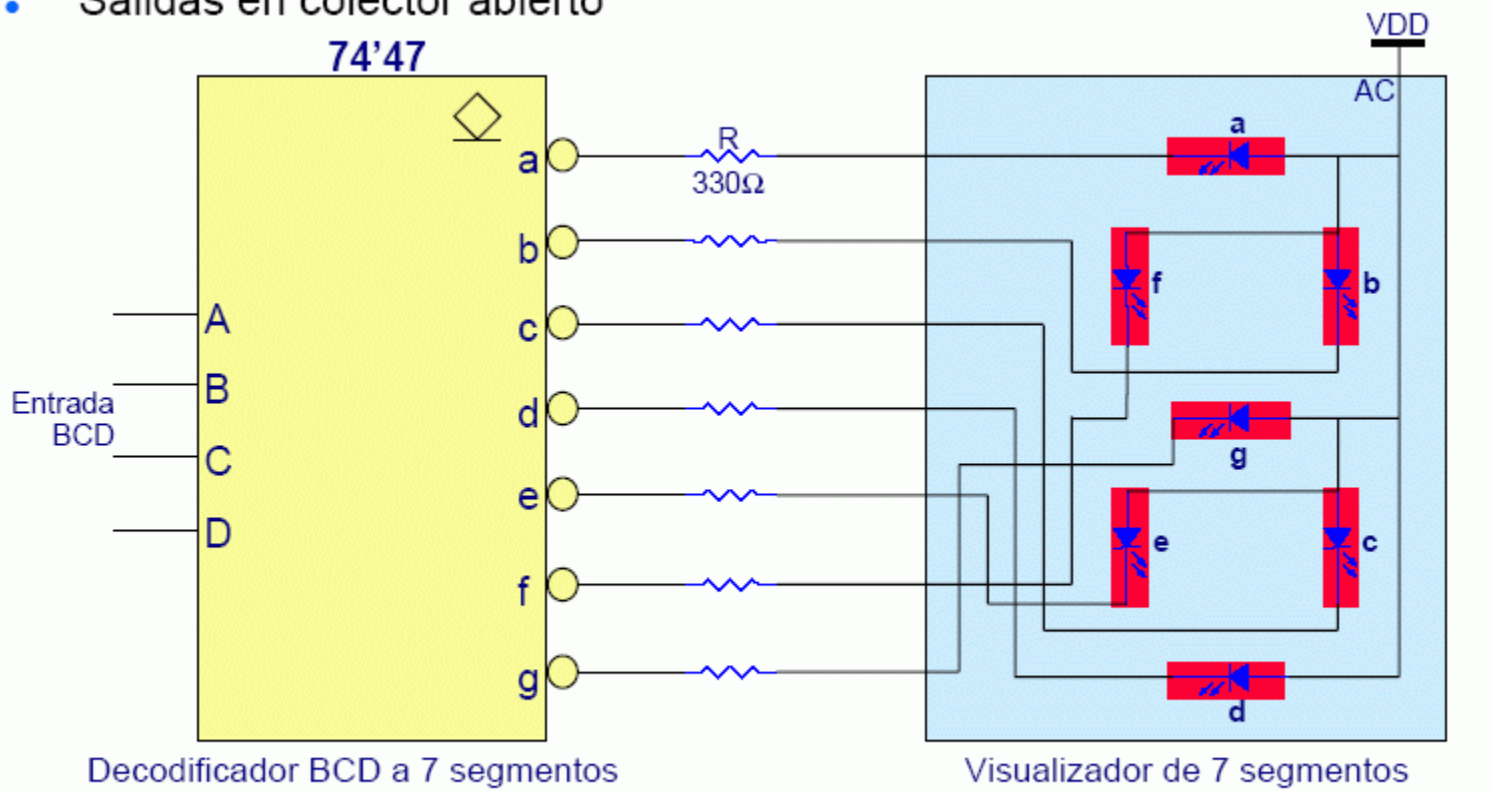
LOGIC SYMBOL

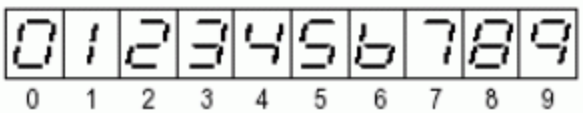


V_{CC} = PIN 16
GND = PIN 8

DEC Display 7

- Salidas en colector abierto





MOTOROLA

BCD TO 7-SEGMENT DECODER/DRIVER

The SN54/74LS47 are Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-IN-

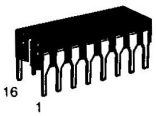
A, B, C, D	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{RBI}$	Ripple-Blanking Input	0.5 U.L.	0.25 U.L.
$\overline{LT}$	Lamp-Test Input	0.5 U.L.	0.25 U.L.
$\overline{BI}/\overline{RBO}$	Blanking Input or Ripple-Blanking Output	0.5 U.L. 1.2 U.L.	0.75 U.L. 2.0 U.L.
$\overline{a}$, to $\overline{g}$	Outputs	Open-Collector	15 (7.5) U.L.

NOTES:
a) 1 Unit Load (U.L.) = 40 µA HIGH, 1.6 mA LOW.
b) Output current measured at V_{OUT} = 0.5 V
The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges.

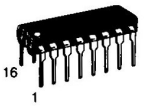
SN54/74LS47

BCD TO 7-SEGMENT DECODER/DRIVER

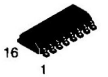
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

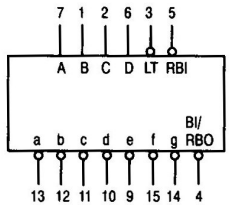


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

MOTOROLA

BCD TO 7-SEGMENT DECODER

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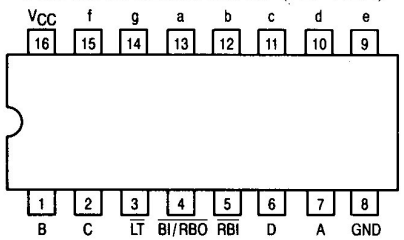
The circuit accepts 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive other components. The relative positive logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables.

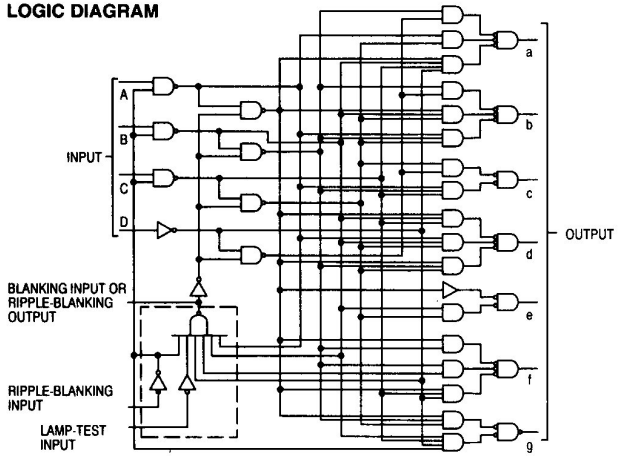
The LS48 circuit incorporates automatic leading and/or trailing edge zero-blanking control (RBI and RBO). Lamp Test (LT) may be activated any time when the BI/RBO node is HIGH. Both devices contain an overriding blanking input (BI) which can be used to control the lamp intensity by varying the frequency and duty cycle of the BI input signal or to inhibit the outputs.

- Lamp Intensity Modulation Capability (BI/RBO)
- Internal Pull-Ups Eliminate Need for External Resistors
- Input Clamp Diodes Eliminate High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC DIAGRAM

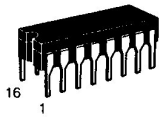


SN54/74LS48

Cátodo comum

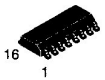
BCD TO 7-SEGMENT DECODER

LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09

N SUFFIX
PLASTIC
CASE 648-08

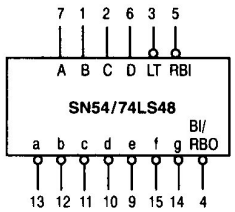


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

ORDERING INFORMATION

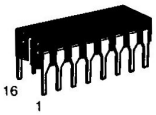
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

SN54/74LS47

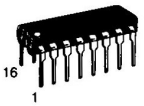
Ânodo comum

BCD TO 7-SEGMENT DECODER/DRIVER

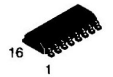
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

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SN74LSXXD	SOIC

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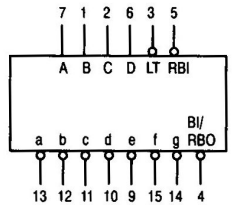

VCC = PIN 16
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OROLA

SEGMENT /DRIVER

ire Low Power Schottky BCD-to-7-Segment Decod-
f NAND gates, input buffers and seven AND-OR-IN-
er active LOW, high sink current outputs for driving
n NAND gates and one driver are connected in pairs
d its complement available to the seven decoding
s. The remaining NAND gate and three input buffers
king input/ripple-blanking output and ripple-blanking

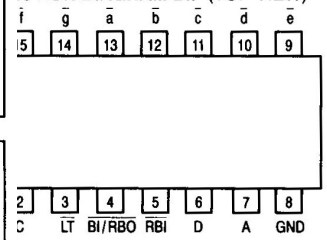
-bit binary-coded-decimal (BCD) and, depending on
inputs, decodes this data to drive a 7-segment display
positive-logic output levels, as well as conditions
ıry inputs, are shown in the truth tables. Output
N54/74LS47 are designed to withstand the relatively
for 7-segment indicators.
withstand 15 V with a maximum reverse current of
ients requiring up to 24 mA of current may be driven
LS47 high performance output transistors. Display
counts above nine are unique symbols to authenticate

ncorporates automatic leading and/or trailing-edge
BI and RBO). Lamp test (LT) may be performed at any
node is a HIGH level. This device also contains an
ut (BI) which can be used to control the lamp intensity
y and duty cycle of the BI input signal or to inhibit the

ilation Capability (BI/RBO)
uts

o Suppression
Limit High-Speed Termination Effects

CTION DIAGRAM DIP (TOP VIEW)

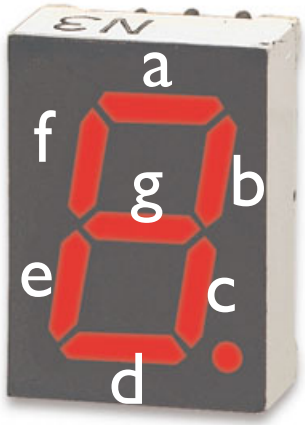


LOADING (Note a)

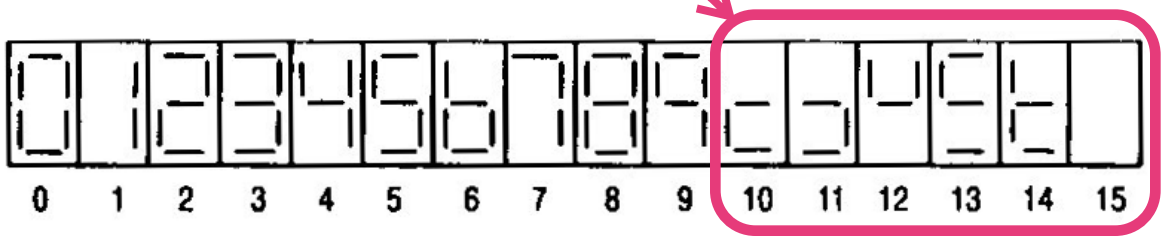
	HIGH	LOW
nputs	0.5 U.L.	0.25 U.L.
-Blanking Input	0.5 U.L.	0.25 U.L.
Test Input	0.5 U.L.	0.25 U.L.
ng Input or	0.5 U.L.	0.75 U.L.
-Blanking Output	1.2 U.L.	2.0 U.L.
ts	Open-Collector	15 (7.5) U.L.

HIGH, 1.6 mA LOW.
t V_{OUT} = 0.5 V
or is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges.

DEC Display 7 Segmentos



Caracteres formados para códigos **BCD** "inválidos"



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

MOTOROLA

BCD TO 7-SEGMENT DECODER

The SN54/74LS48 is a BCD to 7-Segment Decoder consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking input for the LS48.

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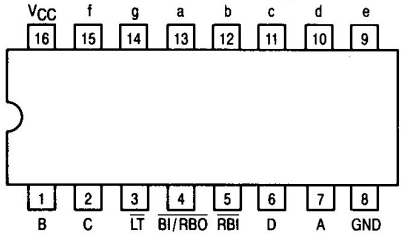
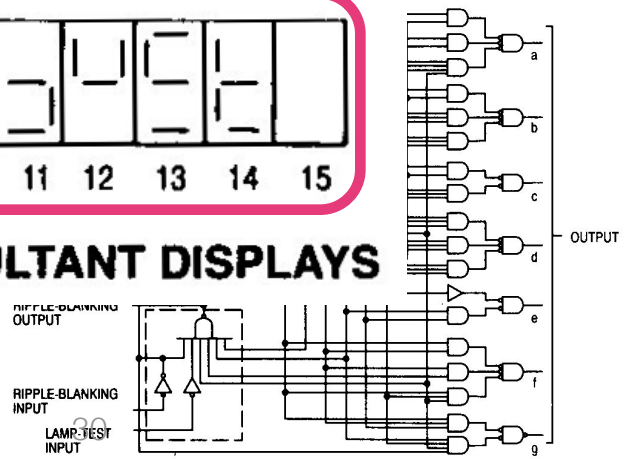
CONNECTION DIAGRAM DIP (TOP VIEW)

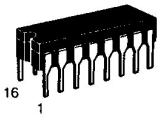




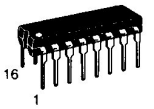
SN54/74LS48

BCD TO 7-SEGMENT DECODER

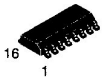
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

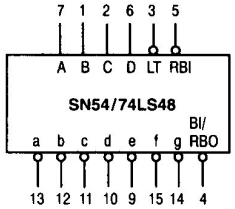


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL

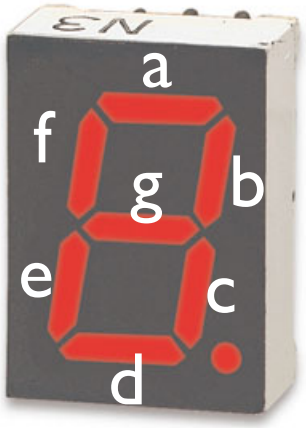


V_{CC} = PIN 16
GND = PIN 8

Condições “Don't care”

- Alguns circuitos possuem certas combinações de entrada para as quais não importa a saída do circuito (ou não existe especificação do nível lógico de saída).
- Ou seja, certas combinações de entradas que não geram impacto na função lógica (a saída pode ir tanto para nível lógico ALTO quanto BAIXO).
- Recebem o nome de termos “don't care”. Na tabela verdade e no mapa, estas condições são registradas usando a letra “X”.
- Exemplo: (segue)...

DEC Display 7 Segmentos/BCD



DECIMAL	BCD
	8421
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

www.electronicsarea.com

Digit Shown	Illuminated Segment (1 = illumination)						
	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	0	1	0	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

Decimal	Entradas				Saídas						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1		1	1				
2	0	0	1	0	1	1		1	1		1
3	0	0	1	1	1	1	1	1			1
4	0	1	0	0		1	1			1	1
5	0	1	0	1	1		1	1		1	1
6	0	1	1	0	1		1	1	1	1	1
7	0	1	1	1	1	1	1				
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1			1	1
10	1	0	1	0	X	X	X	X	X	X	X
11	1	0	1	1	X	X	X	X	X	X	X
12	1	1	0	0	X	X	X	X	X	X	X
13	1	1	0	1	X	X	X	X	X	X	X
14	1	1	1	0	X	X	X	X	X	X	X
15	1	1	1	1	X	X	X	X	X	X	X

Condições “don’t care”

DEC Display 7 Segmentos/BCD

Decimal	Entradas				Saídas						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1		1	1				
2	0	0	1	0	1	1		1	1		1
3	0	0	1	1	1	1	1	1			1
4	0	1	0	0		1	1			1	1
5	0	1	0	1	1		1	1		1	1
6	0	1	1	0	1		1	1	1	1	1
7	0	1	1	1	1	1	1				
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1			1	1
10	1	0	1	0	X	X	X	X	X	X	X
11	1	0	1	1	X	X	X	X	X	X	X
12	1	1	0	0	X	X	X	X	X	X	X
13	1	1	0	1	X	X	X	X	X	X	X
14	1	1	1	0	X	X	X	X	X	X	X
15	1	1	1	1	X	X	X	X	X	X	X

Saída = “X” : significa indiferente

Condições indiferentes

Projeto DEC Display 7 Segmentos

D	C	B	A	a	b	c	d	e	f	g	Display
0	0	0	0	1	1	1	1	1	1	0	”0”
0	0	0	1	0	1	1	0	0	0	0	”1”
0	0	1	0	1	1	0	1	1	0	1	”2”
0	0	1	1	1	1	1	1	0	0	1	”3”
0	1	0	0	0	1	1	0	0	1	1	”4”
0	1	0	1	1	0	1	1	0	1	1	”5”
0	1	1	0	1	0	1	1	1	1	1	”6”
0	1	1	1	1	1	1	0	0	0	0	”7”
1	0	0	0	1	1	1	1	1	1	1	”8”
1	0	0	1	1	1	1	1	0	1	1	”9”

D	C	B	A	a
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1

Sem “don’t care”:

a:

DC \ BA	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11				
10	1	1		

Com “don’t care”:

a:

DC \ BA	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	X	X	X	X
10	1	1	X	X

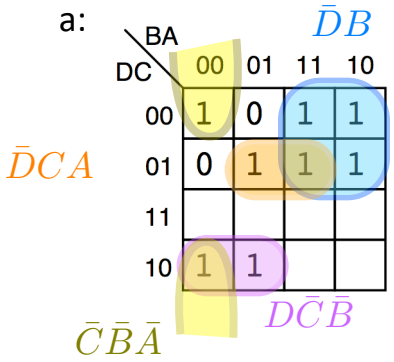
Projeto DEC Display 7 Segmentos

D	C	B	A	a	b	c	d	e	f	g	Display
0	0	0	0	1	1	1	1	1	1	0	”0”
0	0	0	1	0	1	1	0	0	0	0	”1”
0	0	1	0	1	1	0	1	1	0	1	”2”
0	0	1	1	1	1	1	1	0	0	1	”3”
0	1	0	0	0	1	1	0	0	1	1	”4”
0	1	0	1	1	0	1	1	0	1	1	”5”
0	1	1	0	1	0	1	1	1	1	1	”6”
0	1	1	1	1	1	1	0	0	0	0	”7”
1	0	0	0	1	1	1	1	1	1	1	”8”
1	0	0	1	1	1	1	1	0	1	1	”9”

D	C	B	A	a
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1

Sem “don’t care”:

a:

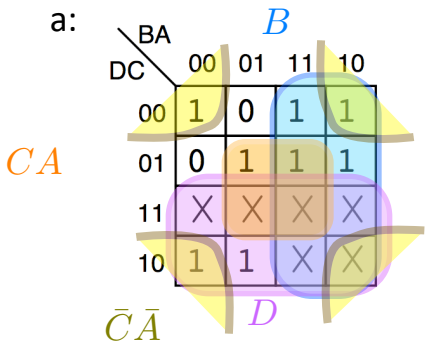


$$a = \bar{D}B + \bar{D}CA + \bar{C}\bar{B}\bar{A} + D\bar{C}\bar{B}$$

1xOR(4)+1xAND(2)+3xAND(3)+4xNOT

Com “don’t care”:

a:



$$a = B + CA + \bar{C}\bar{A} + D$$

1xOR(4)+2xAND(2)+2xNOT

Projeto DEC Display 7 Segmentos

D	C	B	A	a	b	c	d	e	f	g	Display
0	0	0	0	1	1	1	1	1	1	0	”0”
0	0	0	1	0	1	1	0	0	0	0	”1”
0	0	1	0	1	1	0	1	1	0	1	”2”
0	0	1	1	1	1	1	1	0	0	1	”3”
0	1	0	0	0	1	1	0	0	1	1	”4”
0	1	0	1	1	0	1	1	0	1	1	”5”
0	1	1	0	1	0	1	1	1	1	1	”6”
0	1	1	1	1	1	1	0	0	0	0	”7”
1	0	0	0	1	1	1	1	1	1	1	”8”
1	0	0	1	1	1	1	1	0	1	1	”9”

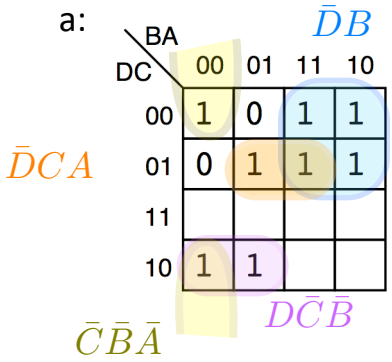
Desvantagem:
- Segmento “a” acende também para códigos não-BCD (ou códigos BCD inválidos)!
- Juntar este “sintoma” ao que acontecerá com os outros segmentos

=> formação de caracteres estranhos para códigos BCD inválidos!

D	C	B	A	a
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1

Sem “don’t care”:

a:

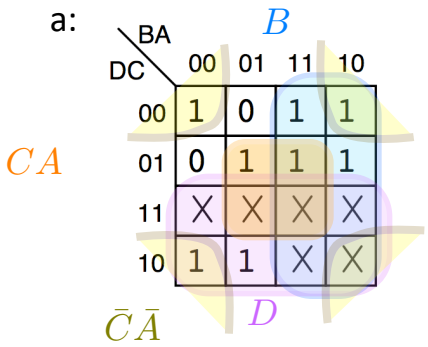


$$a = \bar{D}B + \bar{D}CA + \bar{C}\bar{B}\bar{A} + D\bar{C}\bar{B}$$

1xOR(4)+1xAND(2)+3xAND(3)+4xNOT

Com “don’t care”:

a:

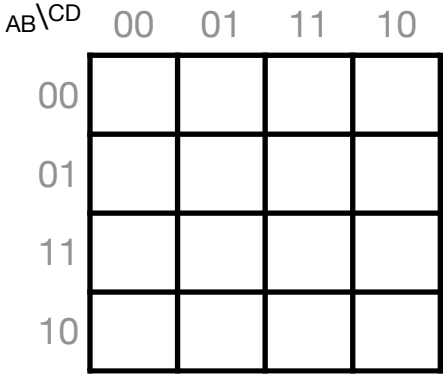


$$a = B + CA + \bar{C}\bar{A} + D$$

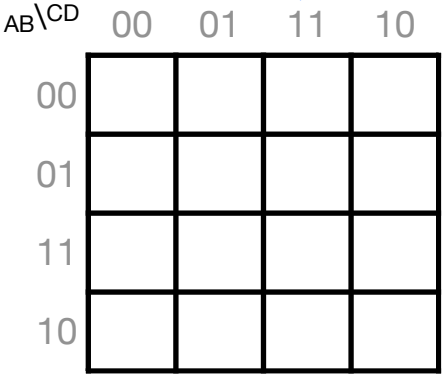
1xOR(4)+2xAND(2)+2xNOT

Projeto DEC Display 7 Segmentos

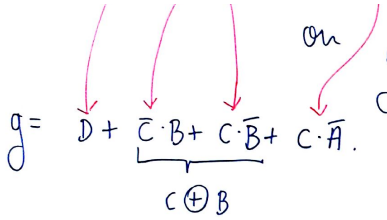
D	C	B	A	a	b	c	d	e	f	g	Display
0	0	0	0	1	1	1	1	1	1	0	”0”
0	0	0	1	0	1	1	0	0	0	0	”1”
0	0	1	0	1	1	0	1	1	0	1	”2”
0	0	1	1	1	1	1	1	0	0	1	”3”
0	1	0	0	0	1	1	0	0	1	1	”4”
0	1	0	1	1	0	1	1	0	1	1	”5”
0	1	1	0	1	0	1	1	1	1	1	”6”
0	1	1	1	1	1	1	0	0	0	0	”7”
1	0	0	0	1	1	1	1	1	1	1	”8”
1	0	0	1	1	1	1	1	0	1	1	”9”



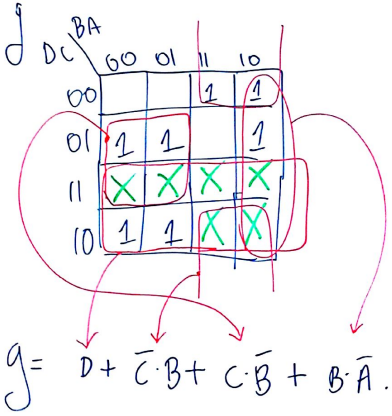
Com “don’t care”:



$e = \bar{C}\cdot\bar{A} + B\cdot\bar{A}$ //



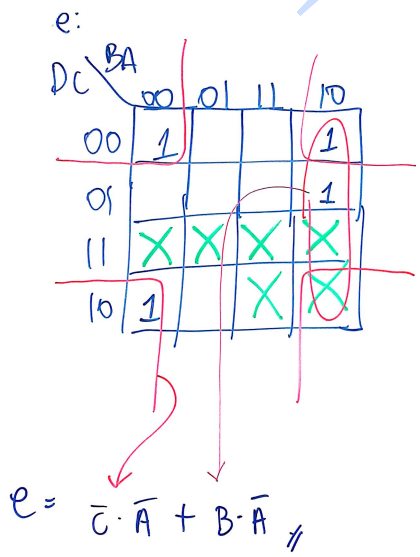
ou

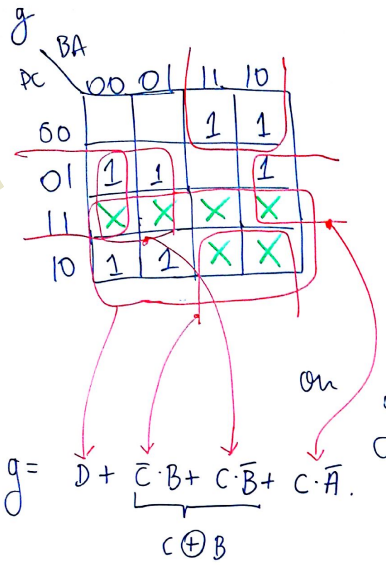


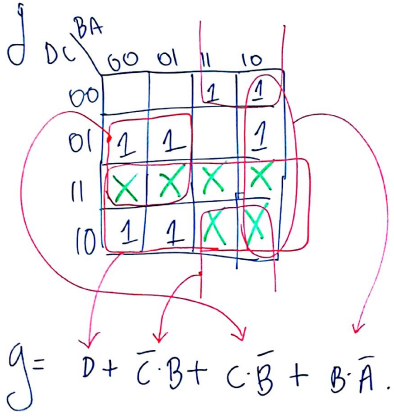
Projeto DEC Display 7 Segmentos

D	C	B	A	a	b	c	d	e	f	g	Display
0	0	0	0	1	1	1	1	1	1	0	”0”
0	0	0	1	0	1	1	0	0	0	0	”1”
0	0	1	0	1	1	0	1	1	0	1	”2”
0	0	1	1	1	1	1	1	0	0	1	”3”
0	1	0	0	0	1	1	0	0	1	1	”4”
0	1	0	1	1	0	1	1	0	1	1	”5”
0	1	1	0	1	0	1	1	1	1	1	”6”
0	1	1	1	1	1	1	0	0	0	0	”7”
1	0	0	0	1	1	1	1	1	1	1	”8”
1	0	0	1	1	1	1	1	0	1	1	”9”

Com “don’t care”:

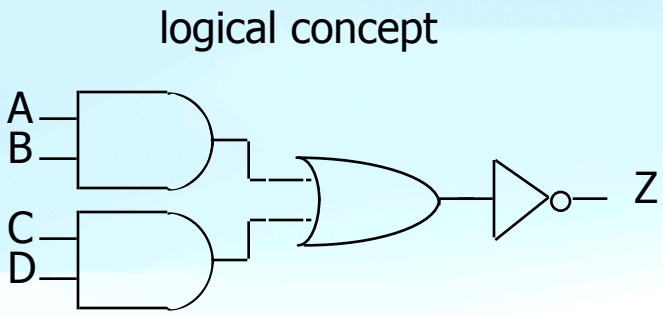


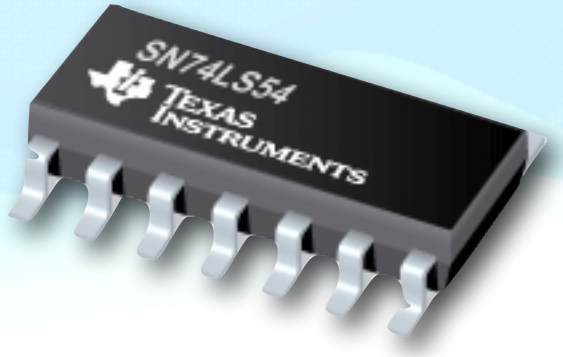




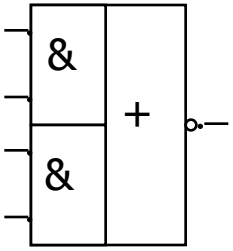
USO de AOIs para Implementar Funções

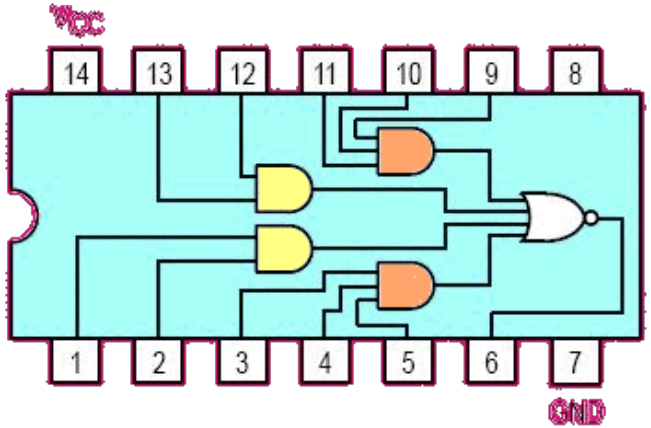
- AOI = And + Or + Inverter (NOT):





2x2 AOI gate symbol





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USO de AOIs para Implementar Funções

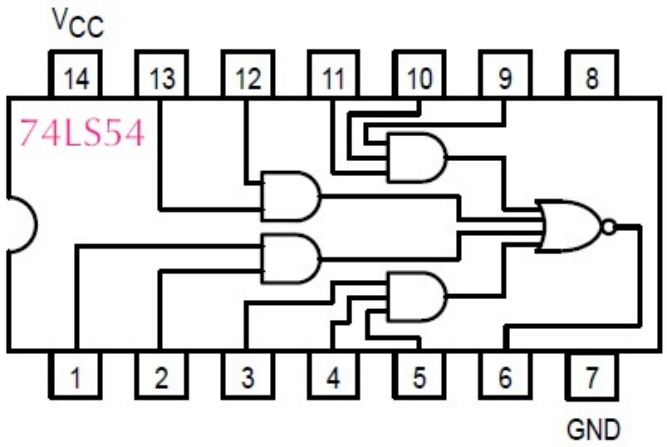
- Exemplo: $a = B + CA + \bar{C}\bar{A} + D$

A •

B •

C •

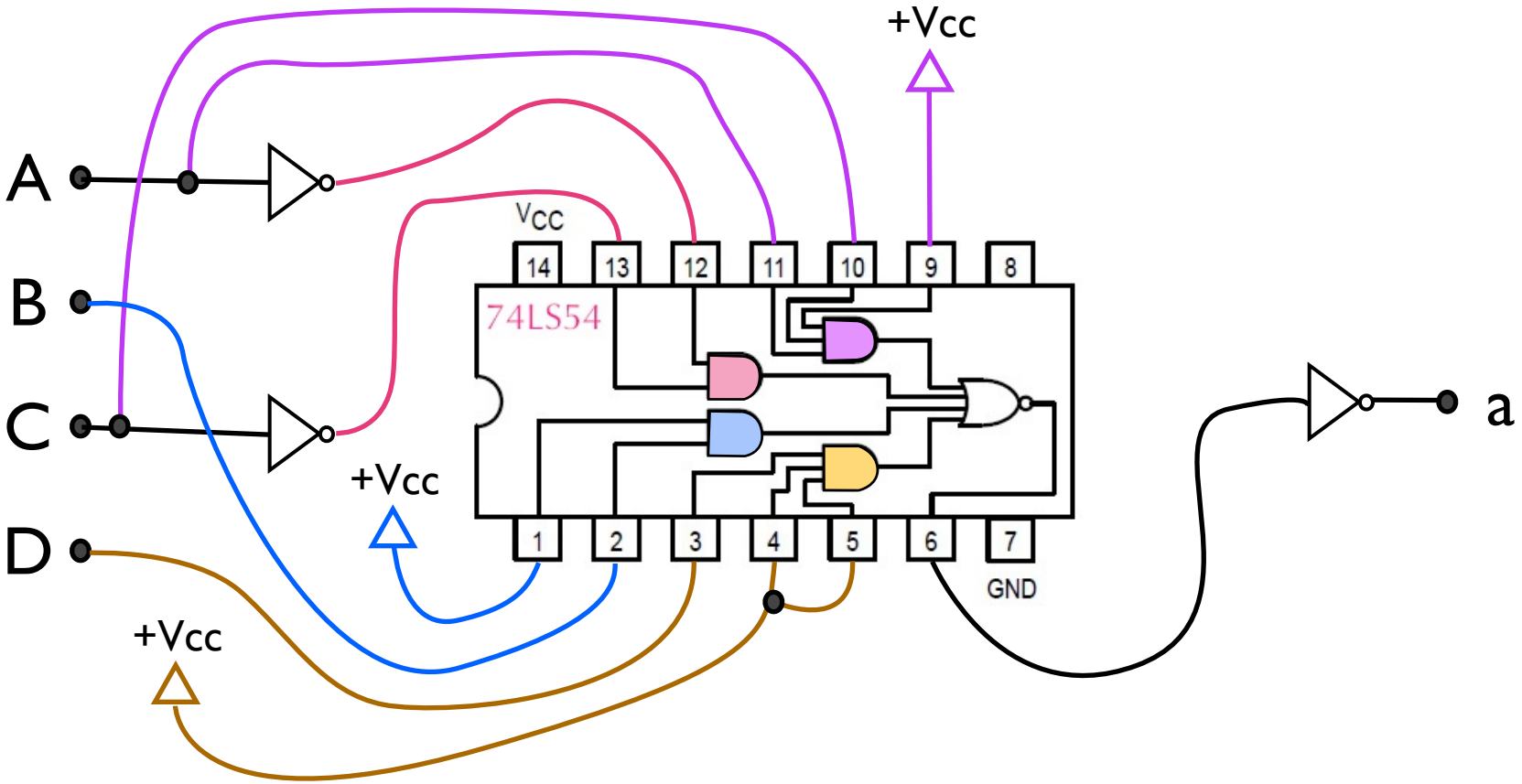
D •



• a

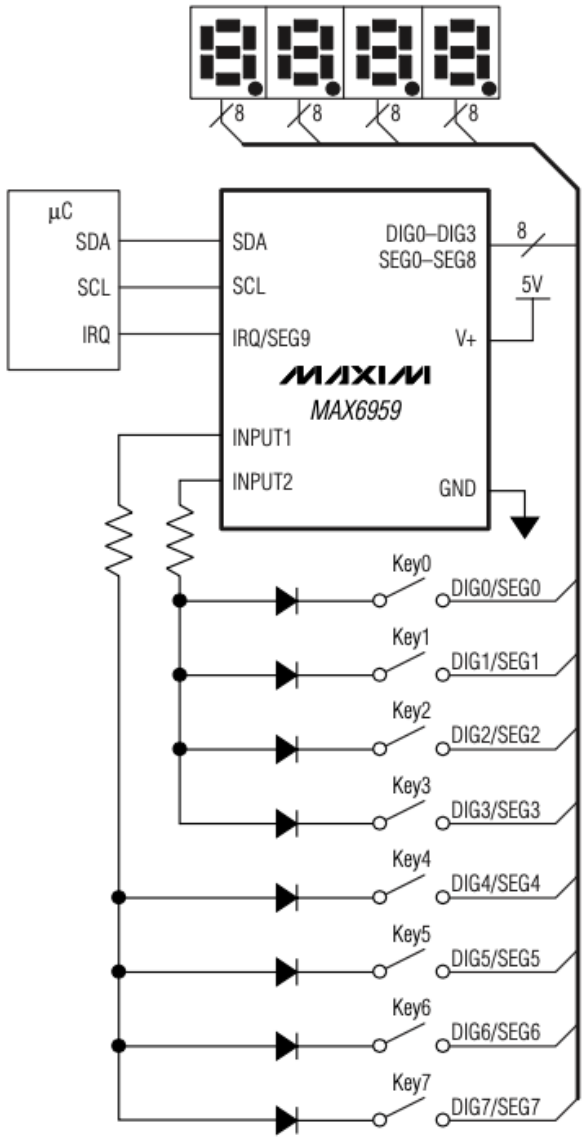
USO de AOIs para Implementar Funções

- Exemplo: $a = B + CA + \bar{C}\bar{A} + D$



Outros DEC Display/Hexa...

- EDE707
- MAX6958/6959:
  Display cátodo comum, 7 ou 9 segmentos;
  Multiplexa até 4 displays;
  I²C (2-wire serial interface);
  Compatível com sistemas de 2,5V e 3,3V
- Hexadecimal-to-Seven Segment Driver:
  MC14495 (CMOS; Motorola; 16 Pin DIP)
- DM9368: 7-Segment Decoder/Driver/Latch
  with Constant Current Source Outputs
- 4311 ou 4368 (CMOS)



Outros DEC Display/Hexa...

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  Display cátodo comum, 7 ou 9 segmentos;
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- Hexadecimal-to-Seven Segment Driver:
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- DM9368: 7-Segment Decoc
  with Constant Current Sourc
- 4311 ou 4368 (CMOS)

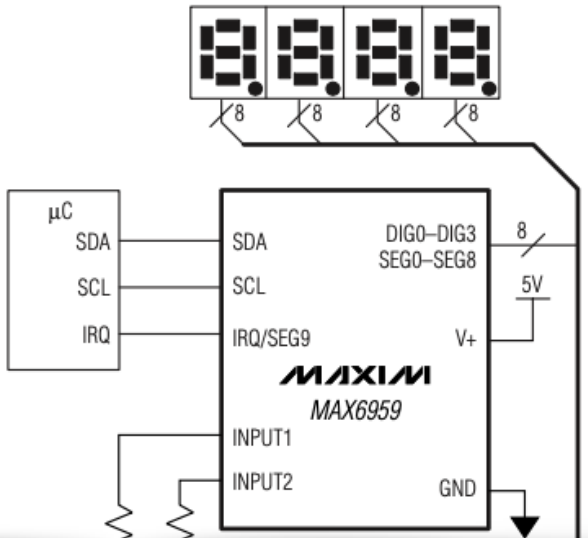


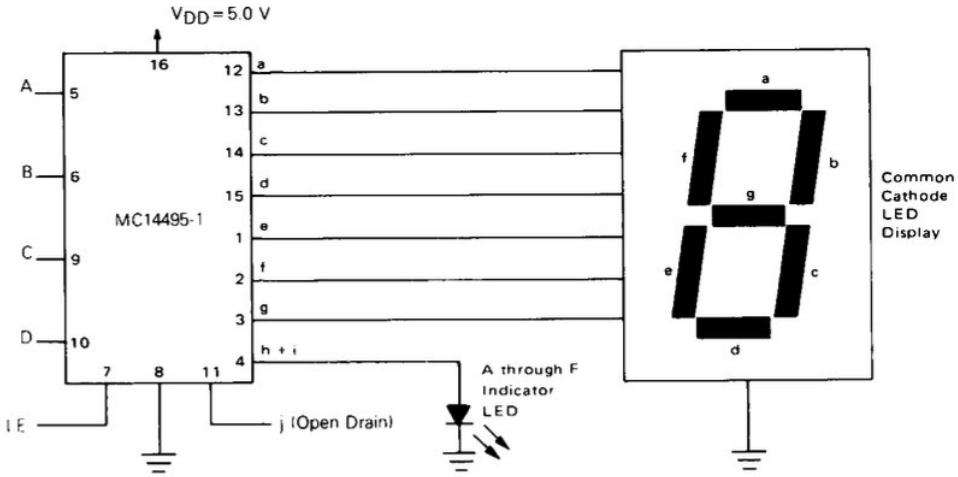
Table 8. Seven-Segment Mapping Decoder for Hexadecimal Font

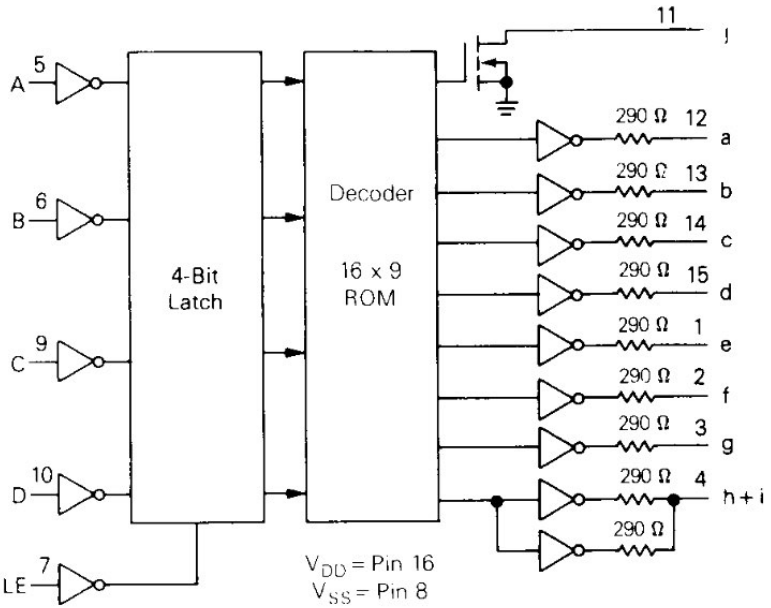
7-SEGMENT CHARACTER	REGISTER DATA					ON SEGMENTS = 1						
	D7–D4	D3	D2	D1	D0	a	b	c	d	e	f	g
0	X	0	0	0	0	1	1	1	1	1	1	0
1	X	0	0	0	1	0	1	1	0	0	0	0
2	X	0	0	1	0	1	1	0	1	1	0	1
3	X	0	0	1	1	1	1	1	1	0	0	1
4	X	0	1	0	0	0	1	1	0	0	1	1
5	X	0	1	0	1	1	0	1	1	0	1	1
6	X	0	1	1	0	1	0	1	1	1	1	1
7	X	0	1	1	1	1	1	1	0	0	0	0
8	X	1	0	0	0	1	1	1	1	1	1	1
9	X	1	0	0	1	1	1	1	1	0	1	1
A	X	1	0	1	0	1	1	1	0	1	1	1
B	X	1	0	1	1	0	0	1	1	1	1	1
C	X	1	1	0	0	1	0	0	1	1	1	0
D	X	1	1	0	1	0	1	1	1	1	0	1
E	X	1	1	1	0	1	0	0	1	1	1	1
F	X	1	1	1	1	1	0	0	0	1	1	1

MAX6958/MAX6959

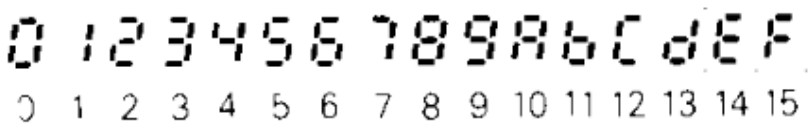
Outros DEC Display/Hexa...

- EDE707
- MAX6958/6959:
  Display cátodo comum, 7 ou 9 segmentos;
  Multiplexa até 4 displays;
  I²C (2-wire serial interface);
  Compatível com sistemas de 2,5V e 3,3V
- Hexadecimal-to-Seven Segment Driver:
  MC14495 (CMOS; Motorola; 16 Pin DIP)
- DM9368: 7-Segment Decoder/Driver/Latch
  with Constant Current Source Outputs
- 4311 ou 4368 (CMOS)



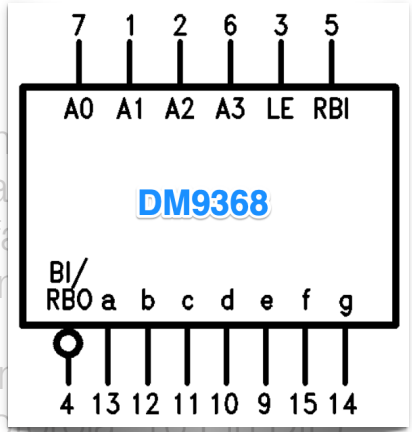


ALPHANUMERIC DISPLAY



Outros DEC Display/Hexa...

- EDE707
- MAX6958/6959:
  Display cátodo comun
  Multiplexa até 4 displa
  I²C (2-wire serial interfa
  Compatível com sister
- Hexadecimal-to-Sever
  MC14495 (CMOS; Mo
- DM9368: 7-Segment Decoder/Driver/Latch with Constant Current Source Outputs



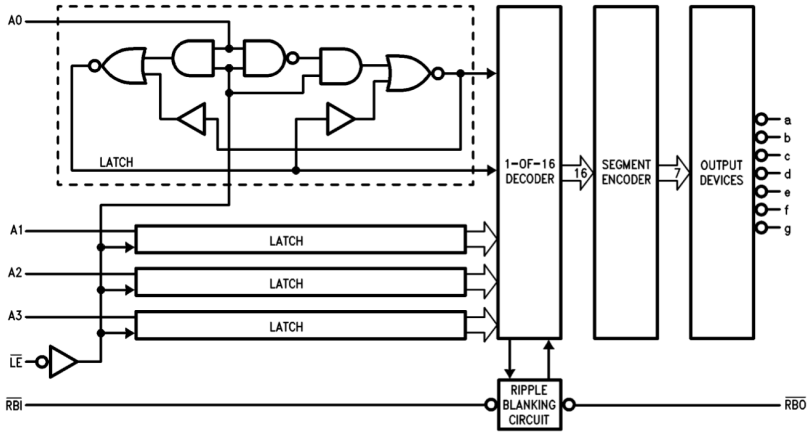
BINARY STATE	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	A3	A2	A1	A0	a	b	c	d	e	f	g	$\overline{RBO}$	
—	H	*	X	X	X	X	← STABLE →							H	STABLE
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
0	L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	H	L	H	H	2
3	L	X	L	L	H	H	H	H	H	H	L	L	H	H	3
4	L	X	L	H	L	L	L	H	H	L	L	H	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	H	H	H	5
6	L	X	L	H	H	L	H	L	H	H	H	H	H	H	6
7	L	X	L	H	H	H	H	H	H	L	L	L	L	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	H	L	L	H	H	H	9
10	L	X	H	L	H	L	H	H	H	L	H	H	H	H	A
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	b
12	L	X	H	H	L	L	H	L	L	H	H	H	L	H	C
13	L	X	H	H	L	H	L	H	H	H	H	L	H	H	d
14	L	X	H	H	H	L	H	L	L	H	H	H	H	H	E
15	L	X	H	H	H	H	H	L	L	L	H	H	H	H	F
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L**	BLANK

TL/F/9796–8

*The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.

**The $\overline{RBO}$ used as an input overrides all other input conditions.

Logic Diagram

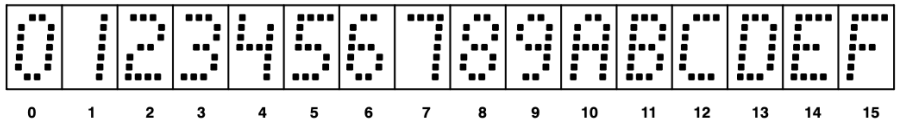


Pin Name	Description
A0–A3	Address (Data) Inputs
$\overline{RBO}$	Ripple Blanking Output (Active Low)
$\overline{RBI}$	Ripple Blanking Input (Active Low)
a–g	Segment Drivers-Outputs
$\overline{LE}$	Latch Enable Input (Active Low)

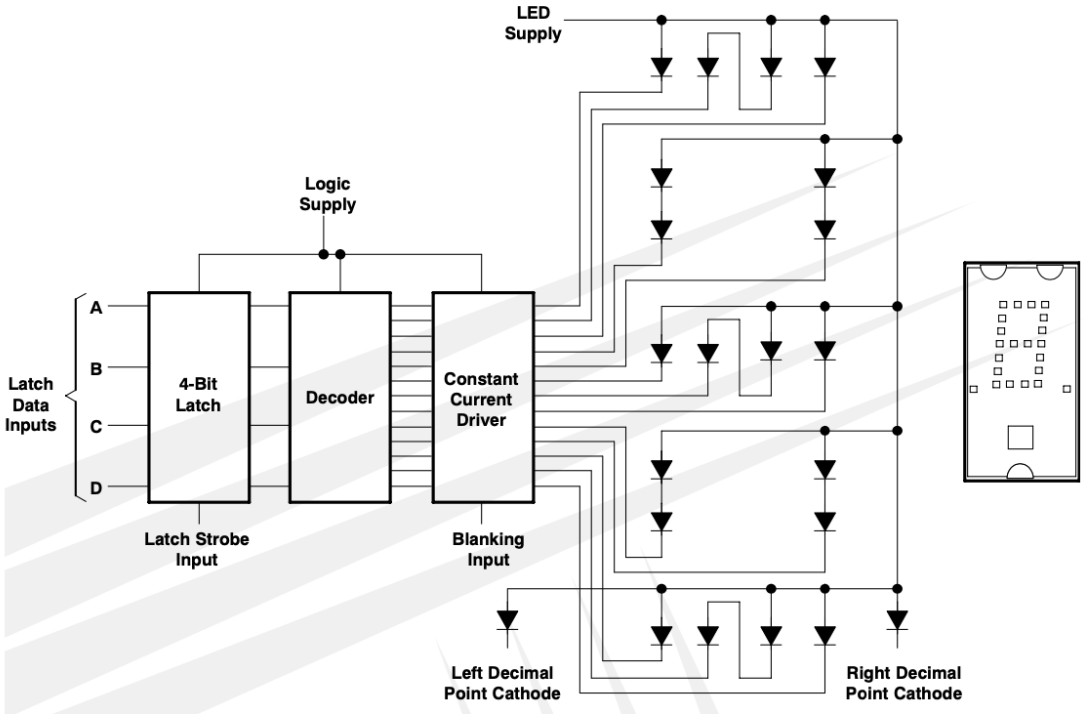
Display HEXA c/DEC

TIL311

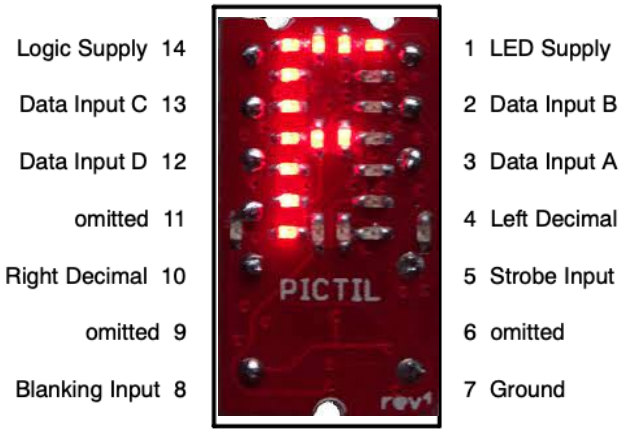
- Internal TTL MSI IC with Latch, Decoder, and Driver
- 0.300-Inch (7,62-mm) Character Height
- Wide Viewing Angle
- High Brightness
- Left-and-Right-Hand Decimals
- Constant-Current Drive for Hexadecimal Characters
- Separate LED and Logic Power Supplies May Be Used
- Operates from 5-V Supply

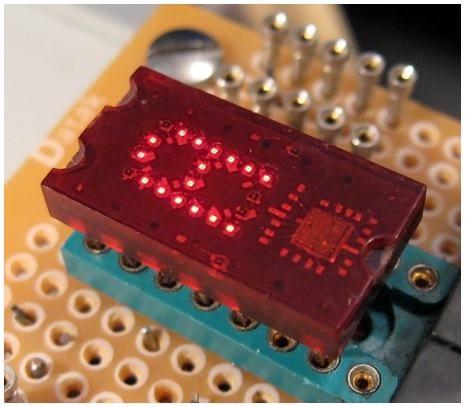


Functional Block Diagram



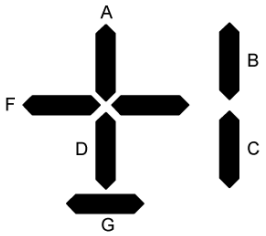
PACKAGE P
14-LEAD PDIP
(BOTTOM VIEW)

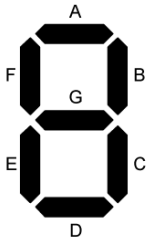




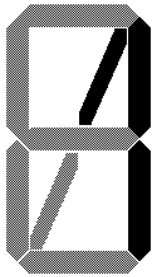
Outros Displays

- 1/2 Display:

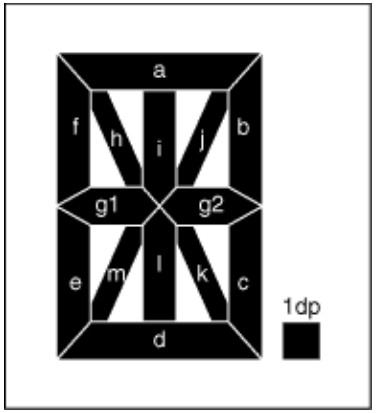




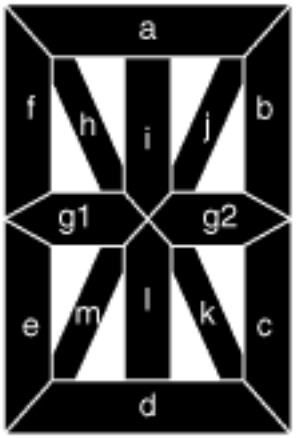
- 9 segmentos:



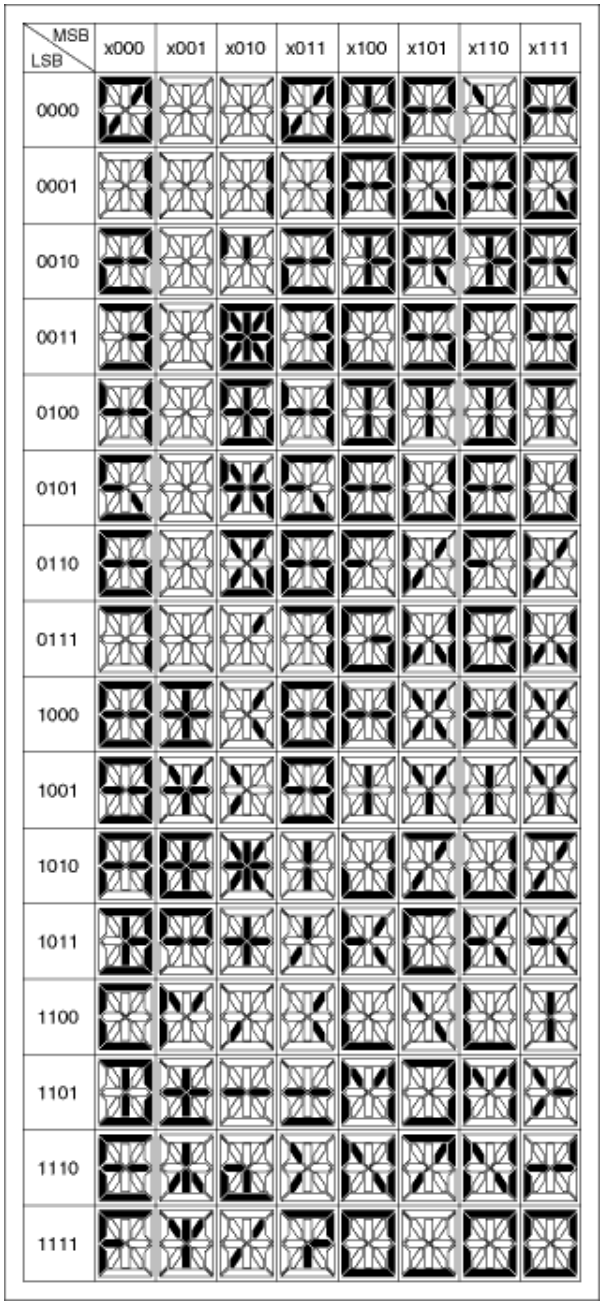
- 14/16 segmentos.



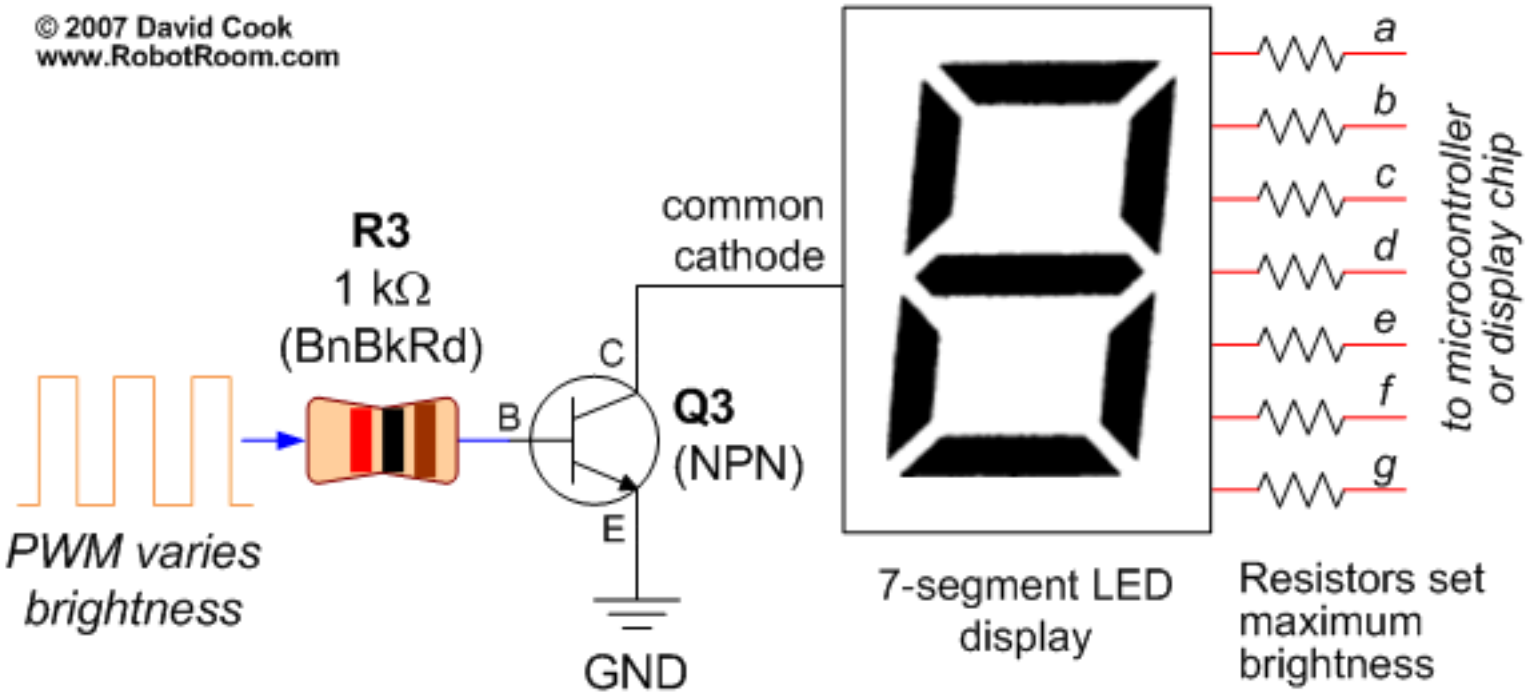
Outros Displays



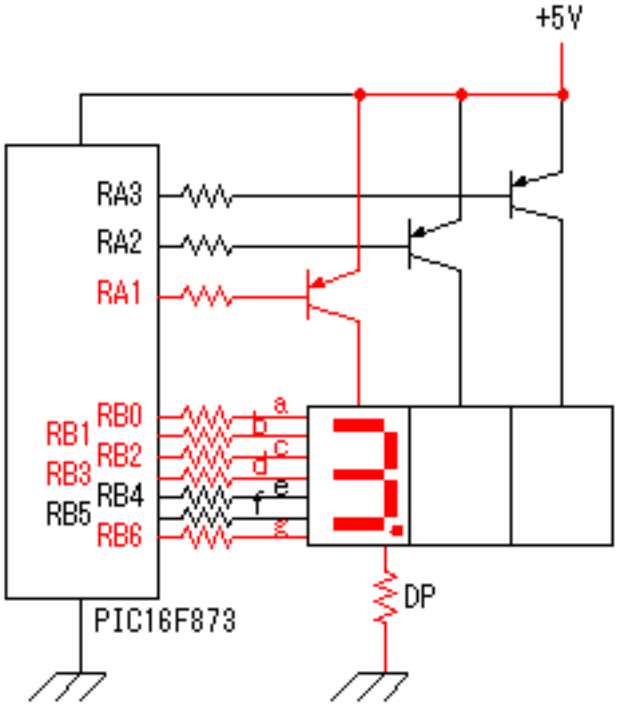
← 14/16 segmentos →



Controlando Brilho Display

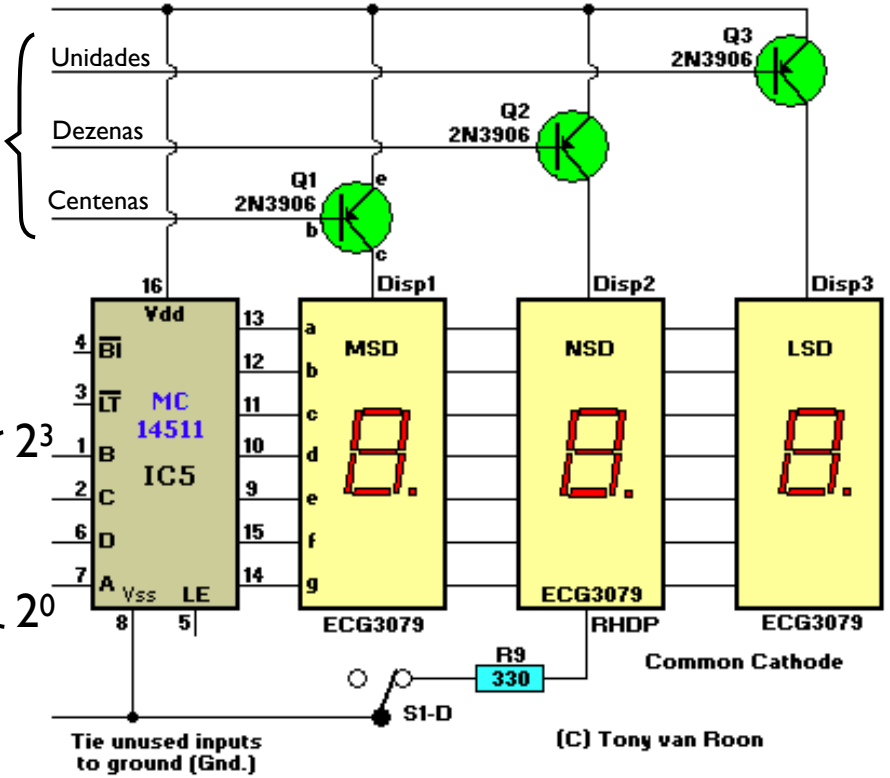


Multiplexação de Displays



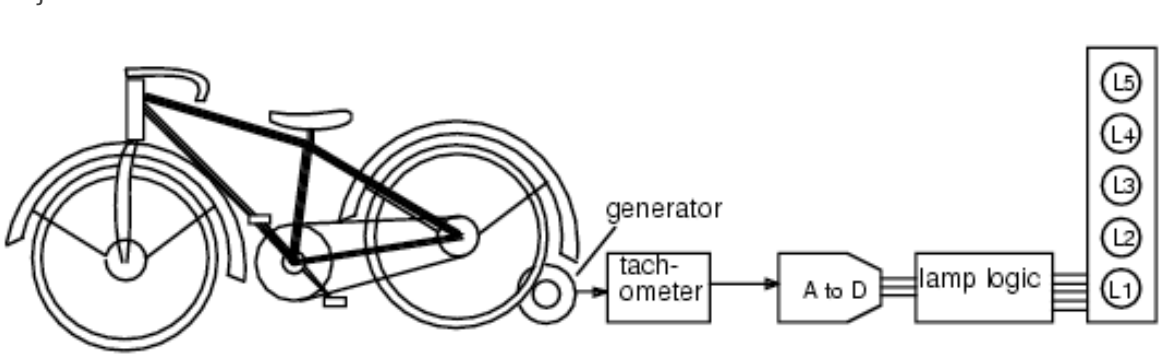
Linhas habilitação de cada display

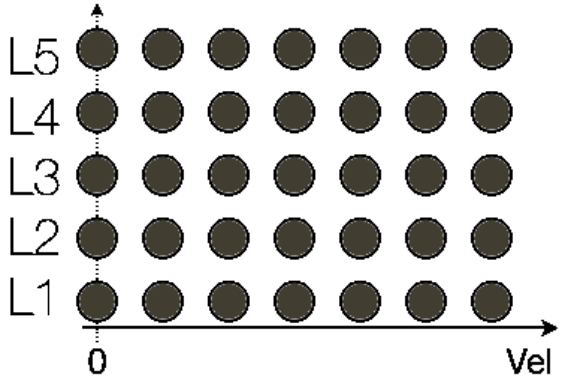
Código BCD



Problema:

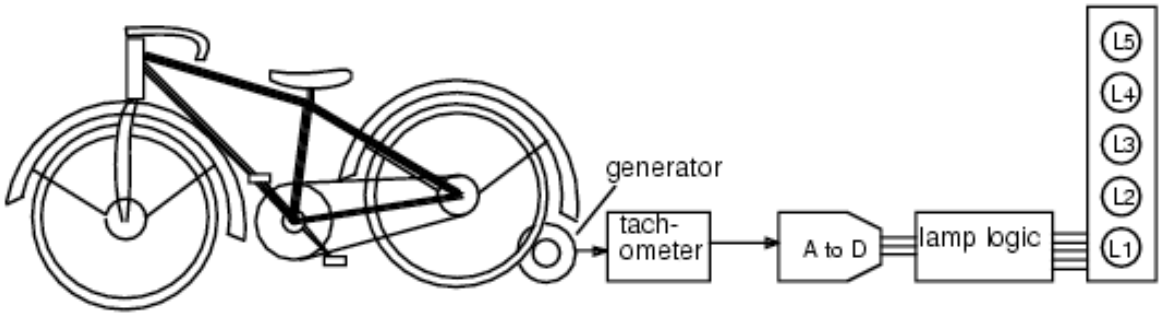
- Projetar um circuito onde o número de leds ativos aumenta conforme aumenta a velocidade da bicicleta.

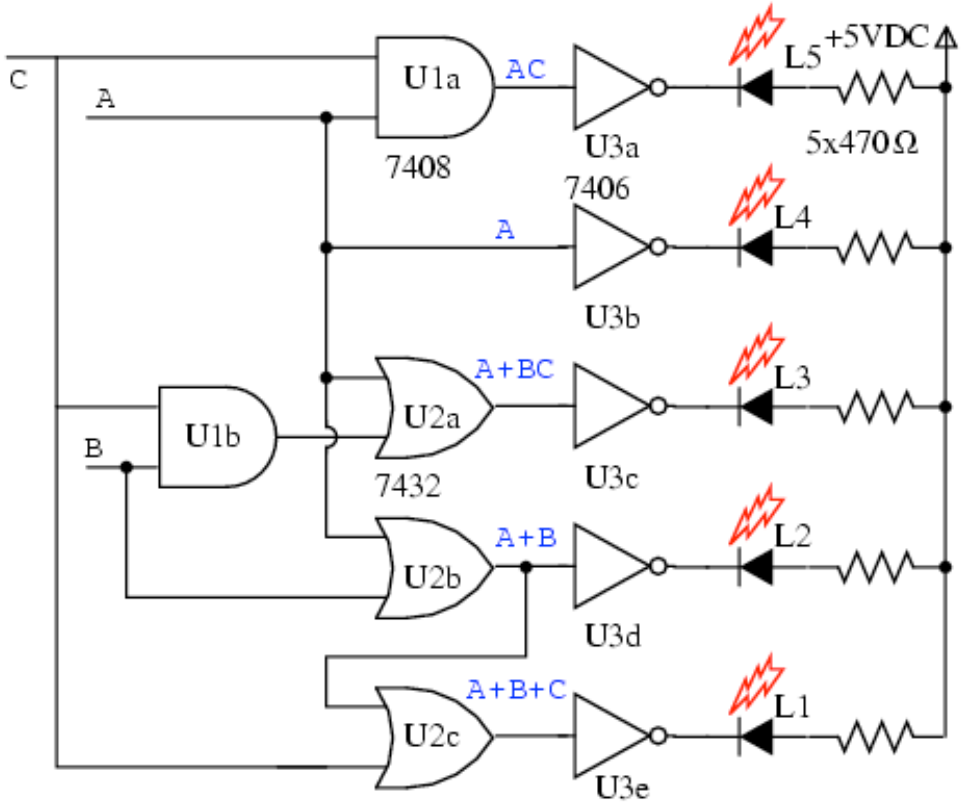




- Neste circuito um pequeno gerador DC acoplado à roda da bicicleta gera uma saída proporcional a velocidade sendo desenvolvida.
- A saída do gerador DC alimenta a placa de um tacogerador que limita sua tensão de saída se o gerador DC ultrapassar certa tensão. Isto é, mesmo que a velocidade da bicicleta aumente além de certa velocidade máxima, a saída do tacogerador já atingiu seu limite e todos os leds já estarão acesos.
- Um conversor A/D de 3-bits converte a tensão do tacogerador para os bits de saída: A, B e C, onde A=MSB e C=LSB.
- Detalhes: o conjunto de 5 leds deve responder para 6 códigos de saída do A/D. Quando ABC=000, bicicleta sem movimento, nenhum led deve se ativar. Para os seguintes 5 códigos de saída: 001 ~ 101 os leds L1, L2, L3, L4 e L5 devem se ativar conforme a velocidade aumenta. Note que não estamos usando os códigos de saída: 110 e 111 porque se supõe que estes códigos nunca ocorrem uma vez que a faixa de excursão de entrada do A/D foi limitada pela placa do tacogerador.

Solução Possível:






You have to fall,
before you can fly